

# IH61F-MHS REV 6.1

## CPU:

Intel Sandy Bridge processors in LGA1155 Package 95W

## System Chipset:

Sugar Point

## Main Memory:

Dual Channel/DDR-III\*2(Max 16GB) 1066/1333

## Onboard Device:

Super I/O:IT8728

LAN:Realtek 8111E

HD Codec:ALC892 3 jacks

PCI BRIDGE:IT8893E

USB3.0 CONTROLLER:NEC uPD720200

## Power solution:

CPU Voltage Regulators:3phase by uP6235 high 1 low 2 OV BY UP6262 MOSFET HEARSINK

AXG voltage Regulators:1phase by uP6235 high 1 low 2

VTT voltage Regulators:1Phase by UP6109 high 1 low 2 OV BY UP6262

DDR voltage Regulators:1Phase by UP6109 high 1 low 1 OV BY UP6262

## Expansion Slots:

PCI EXPRESS 16X SLOT\*2

PCI EXPRESS 1X SLOT\*1

PCI SLOT\*1

## REAR IO:

PS/2 +2 layer USB2.0 Port

HDMI Port

DVI Port

VGA Port

2 layer USB3.0 + Gb RJ-45 Ports

Audio Jacks

## Front I/O:

4SATA2(Red)

USB Header \* 2

CPU /System1/System2 FAN

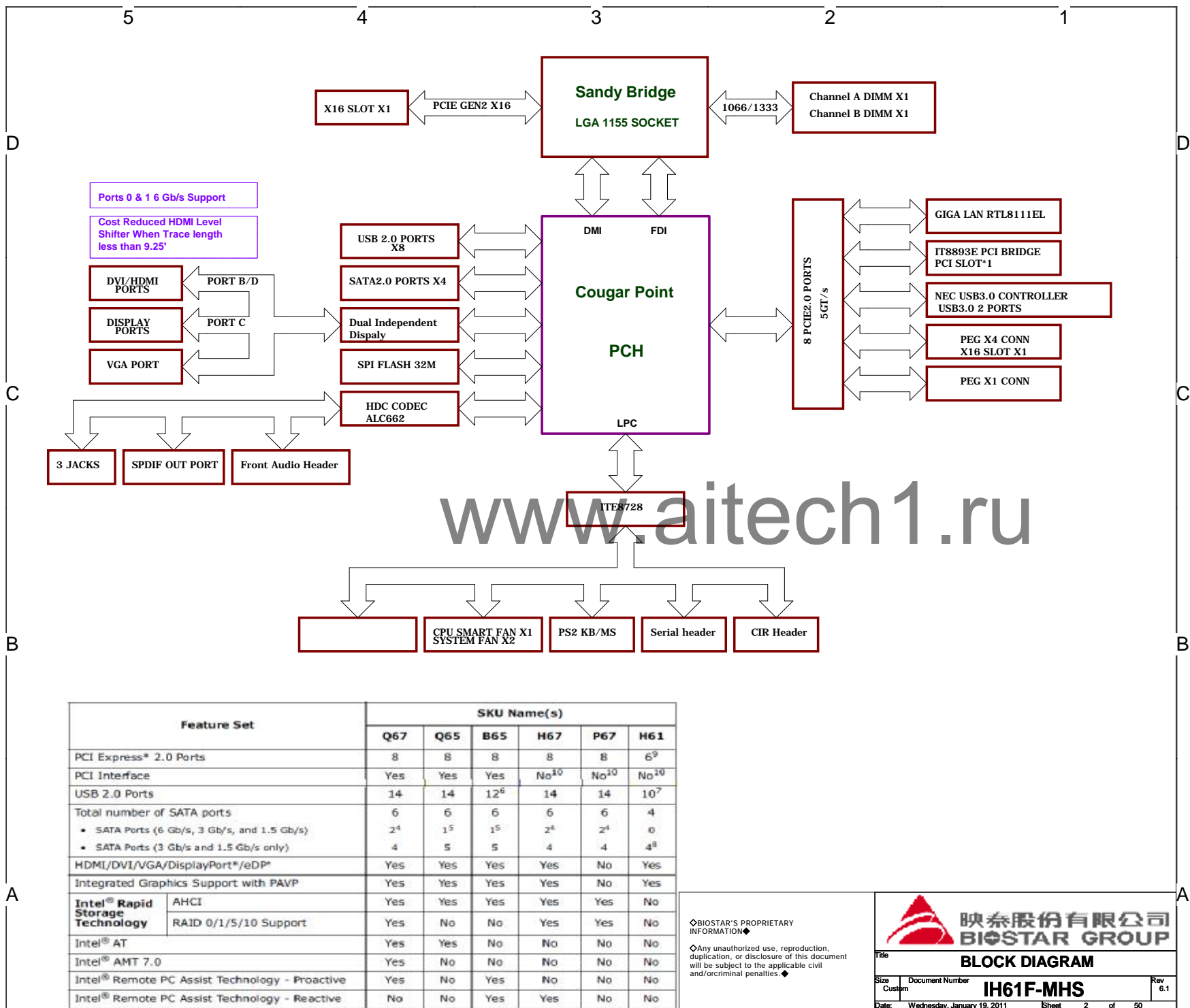
Serial header

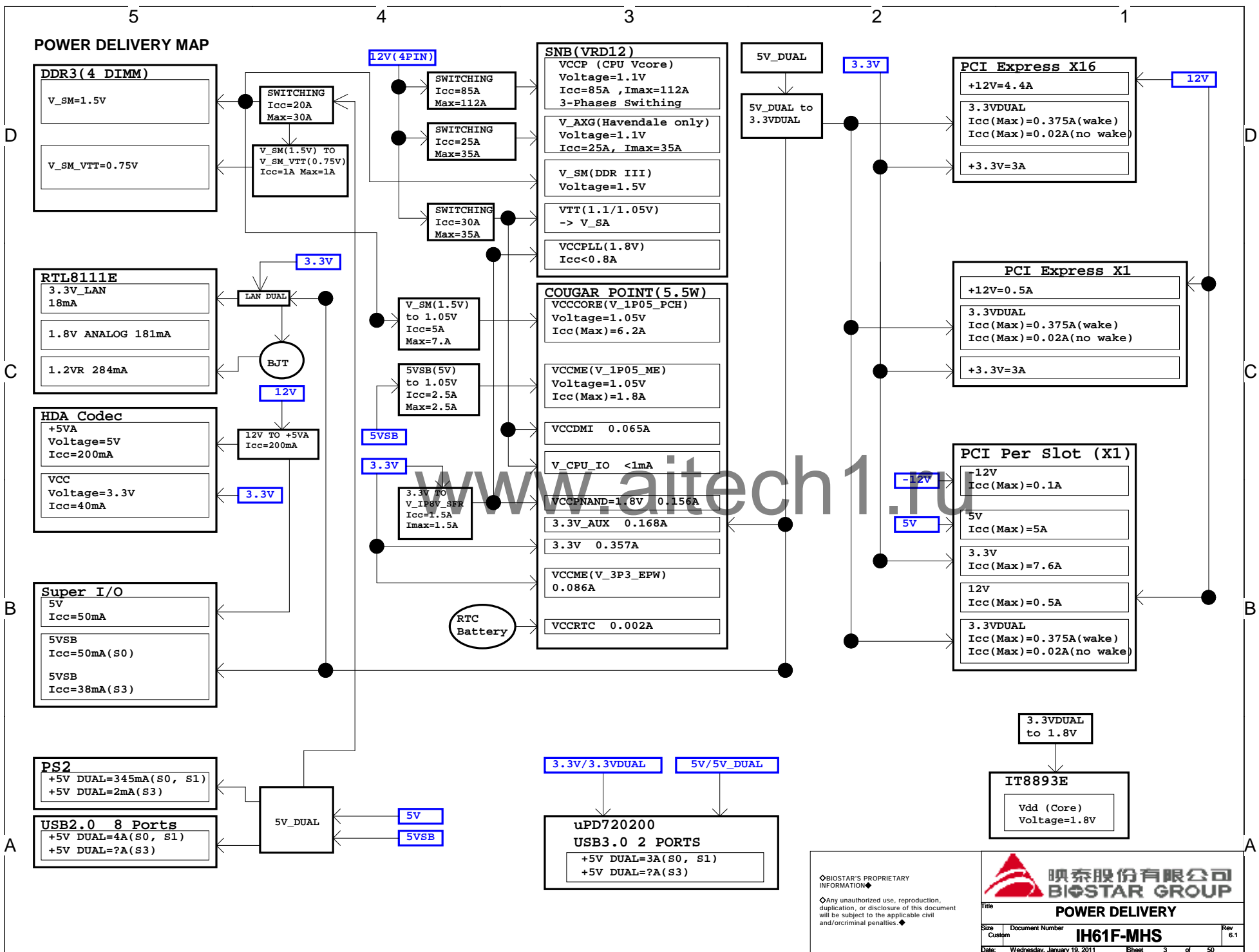
CIR Header

Front Audio Header & SPDIF Out 1

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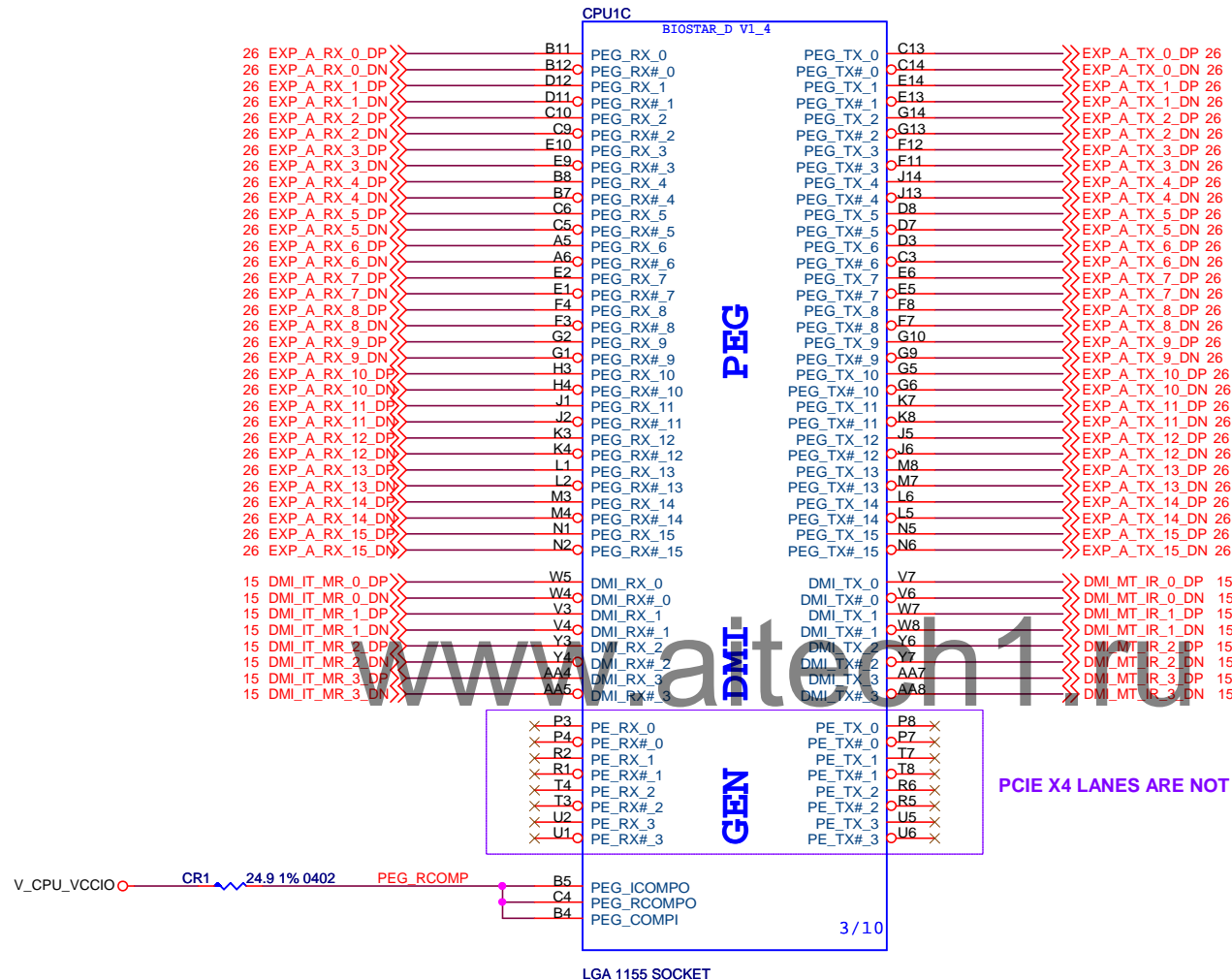
	5	4	3	2	1	
D						D
C						C
B						B
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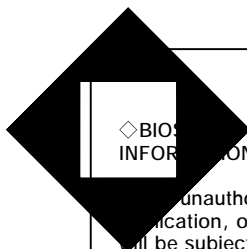
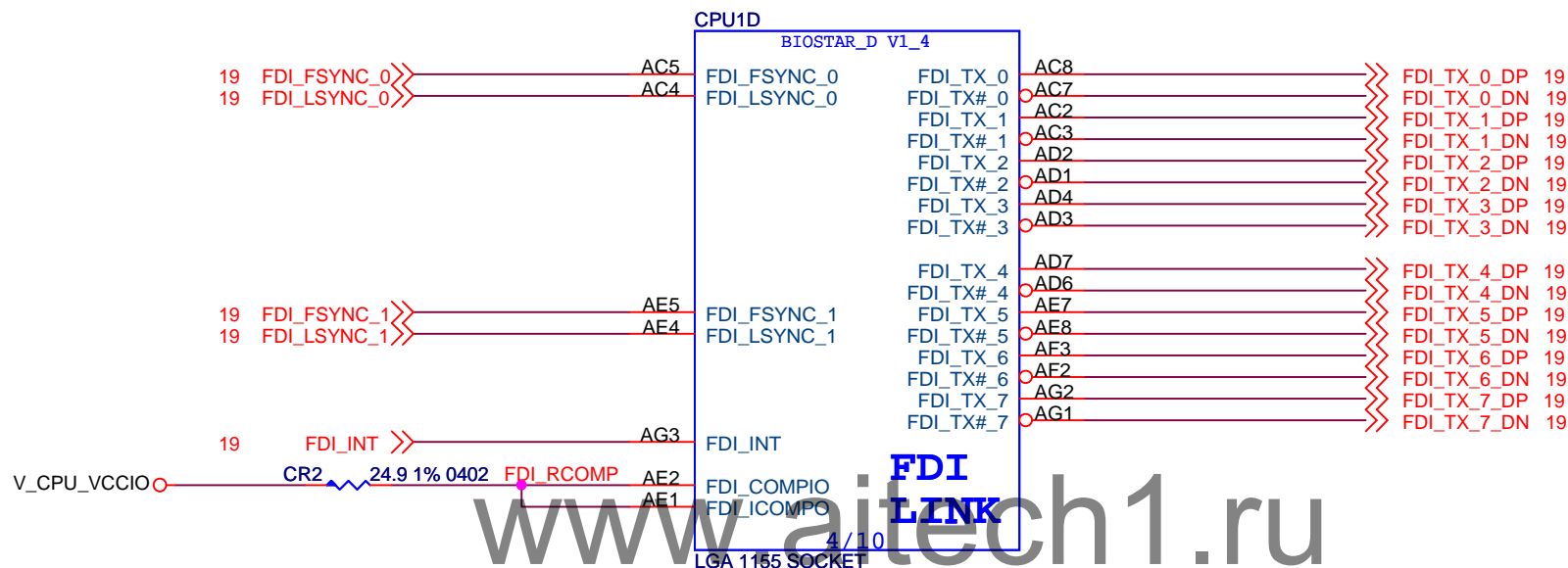
# CPU PART: C+Reference



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Title <b>CPU PCIEX16/DMI</b>			
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# CPU PART: C+Reference



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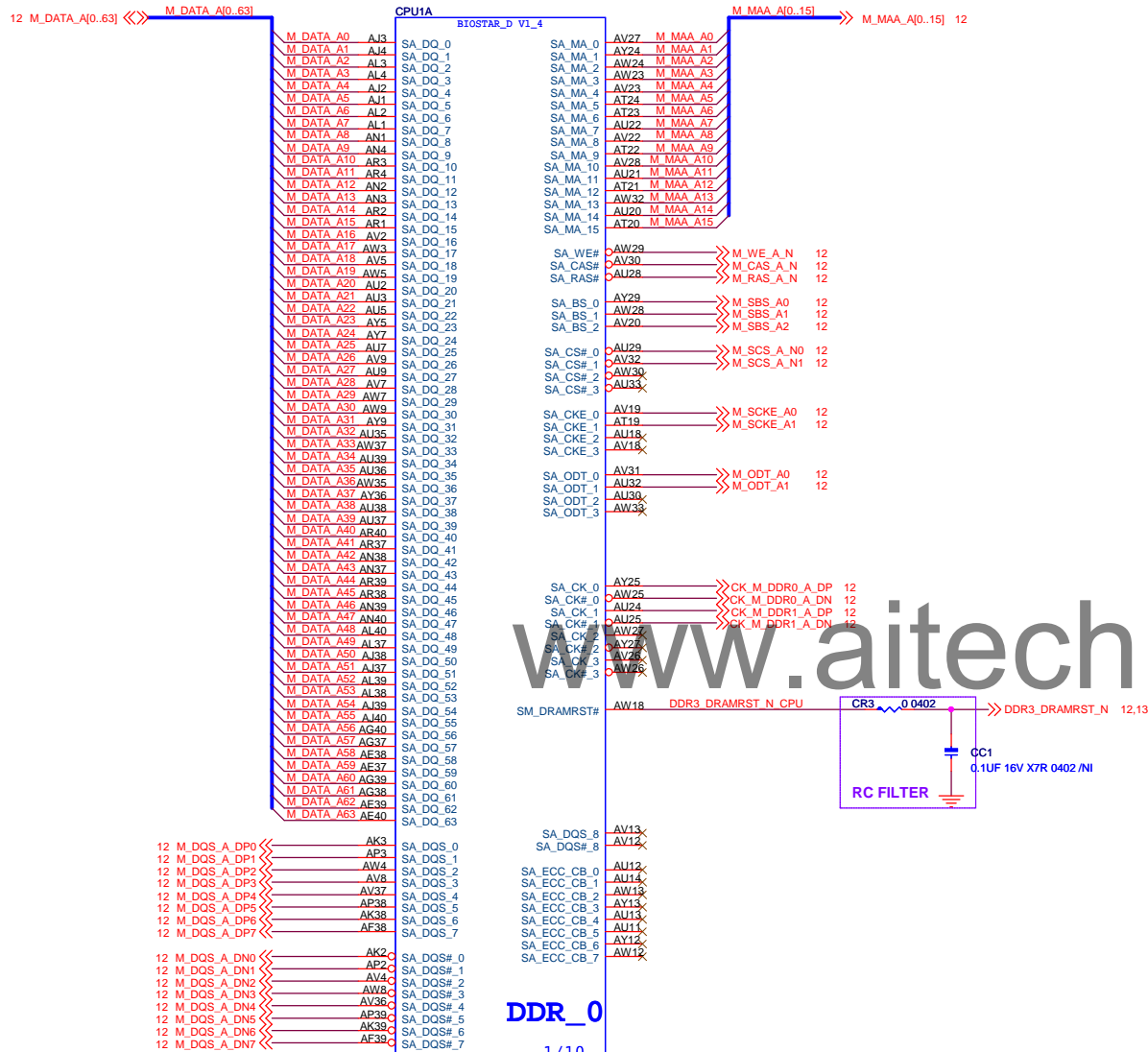
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# CPU PART: C+Reference



LGA 1155 SOCKET

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File			
CPU DDR CHANNEL A			
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[illegible]

DQ REMAPPING IMPLEMENTED  
TO IMPROVE BREAKOUT AND  
MINIMIZE CH-2-CH COUPLING

Q 40  
Q 41  
Q 42  
Q 43  
Q 44 SB CK#0 AL21 >>> CK\_MDDR0\_B\_DP 13  
Q 45 SB CK#0 AL22 >>> CK\_MDDR0\_B\_DN 13  
Q 46 SB CK#1 AL20 >>> CK\_MDDR1\_B\_DP 13  
Q 47 SB CK#1 AL20 >>> CK\_MDDR1\_B\_DN 13  
Q 48 SB CK#2 AL23 >>> CK\_MDDR1\_B\_DN 13

DDR\_1

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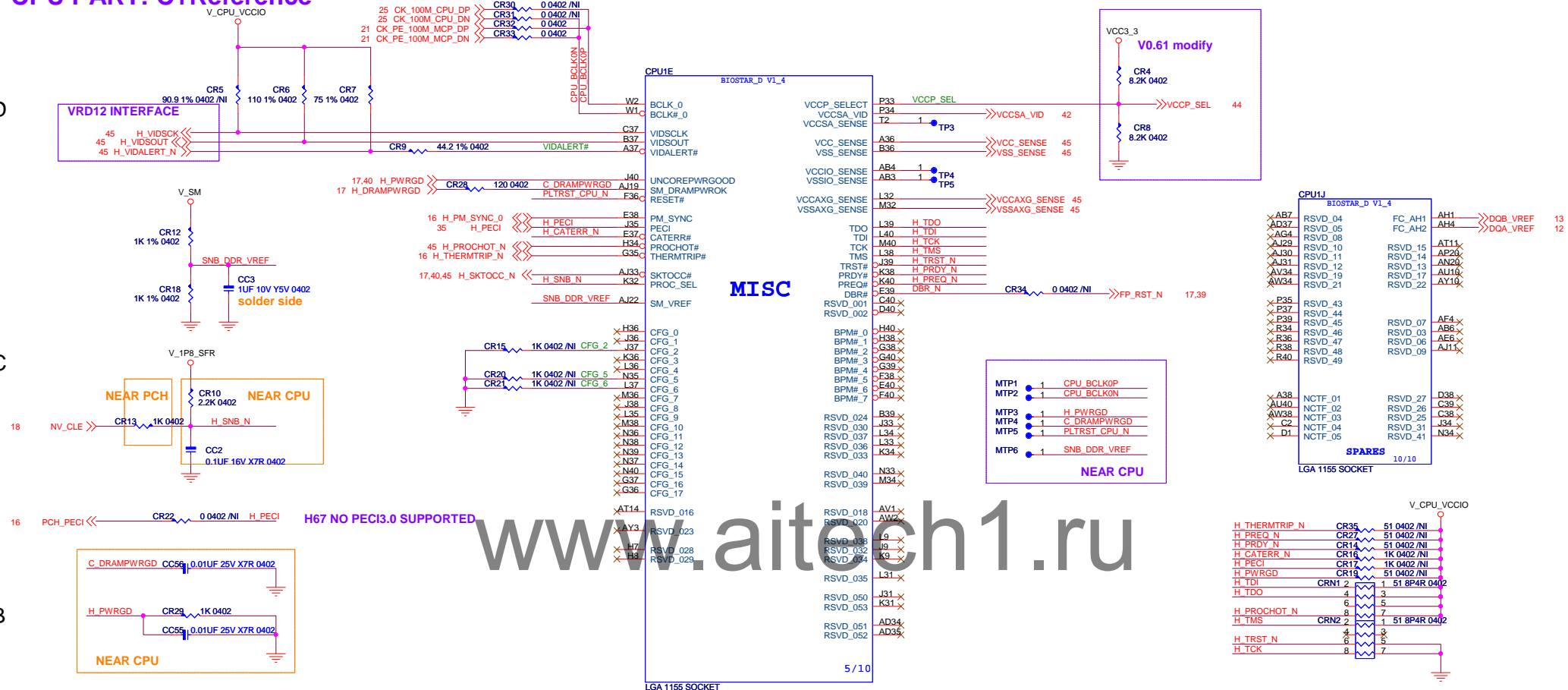
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Title	CPU DDR CHANNEL A
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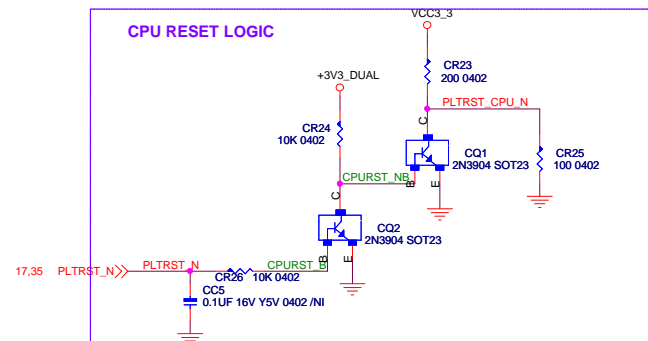
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## CPU PART: C+Reference



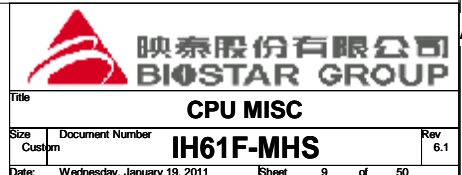
CFG6	CFG5	PCIE CONFIG
1	1	1 X 16
1	0	2 X 8
0	1	RESERVED
0	0	X8,X4,X4

CFG	H	L	DESCRIPTION
2	NORM	RESERVED	PEGLANE REVERSAL[0],X16
5	*	*	SEL0
6	*	*	SEL1



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D

C

B

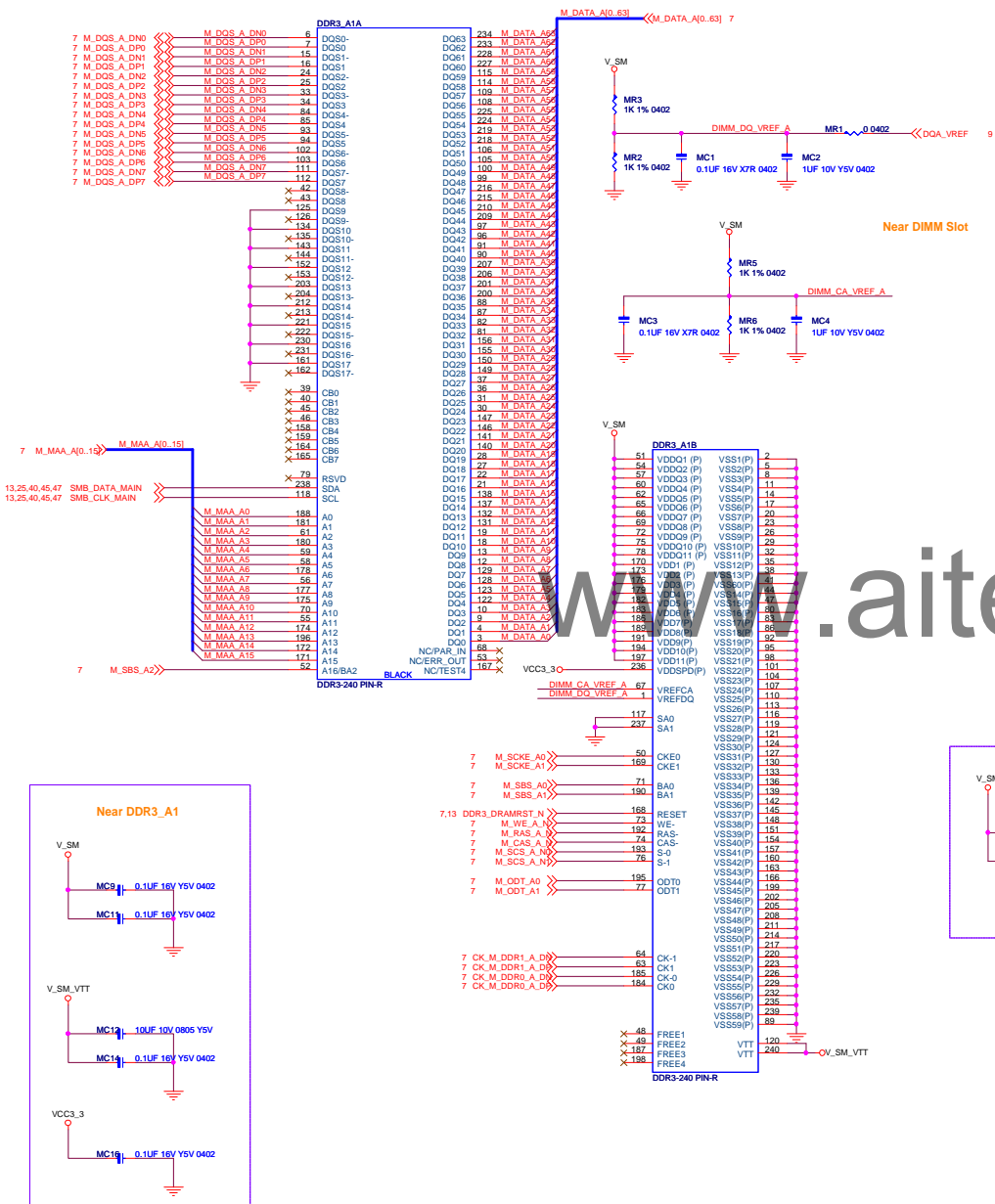
A

D

C

B

A



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File	DDR2 DIMM1A/2		Rev
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**PCH PART: Y+Reference**

**WEAK INTERNAL PULLUPS ON GNT\*.DEFAULT SPI BOOT DEVICE**

GNT1	GNT0/SATA1GP	BOOT DEVICE
0	0	LPC
0	1	NANO
1	0	PCI
1	1	SPI

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**PCH PART: Y+Reference**

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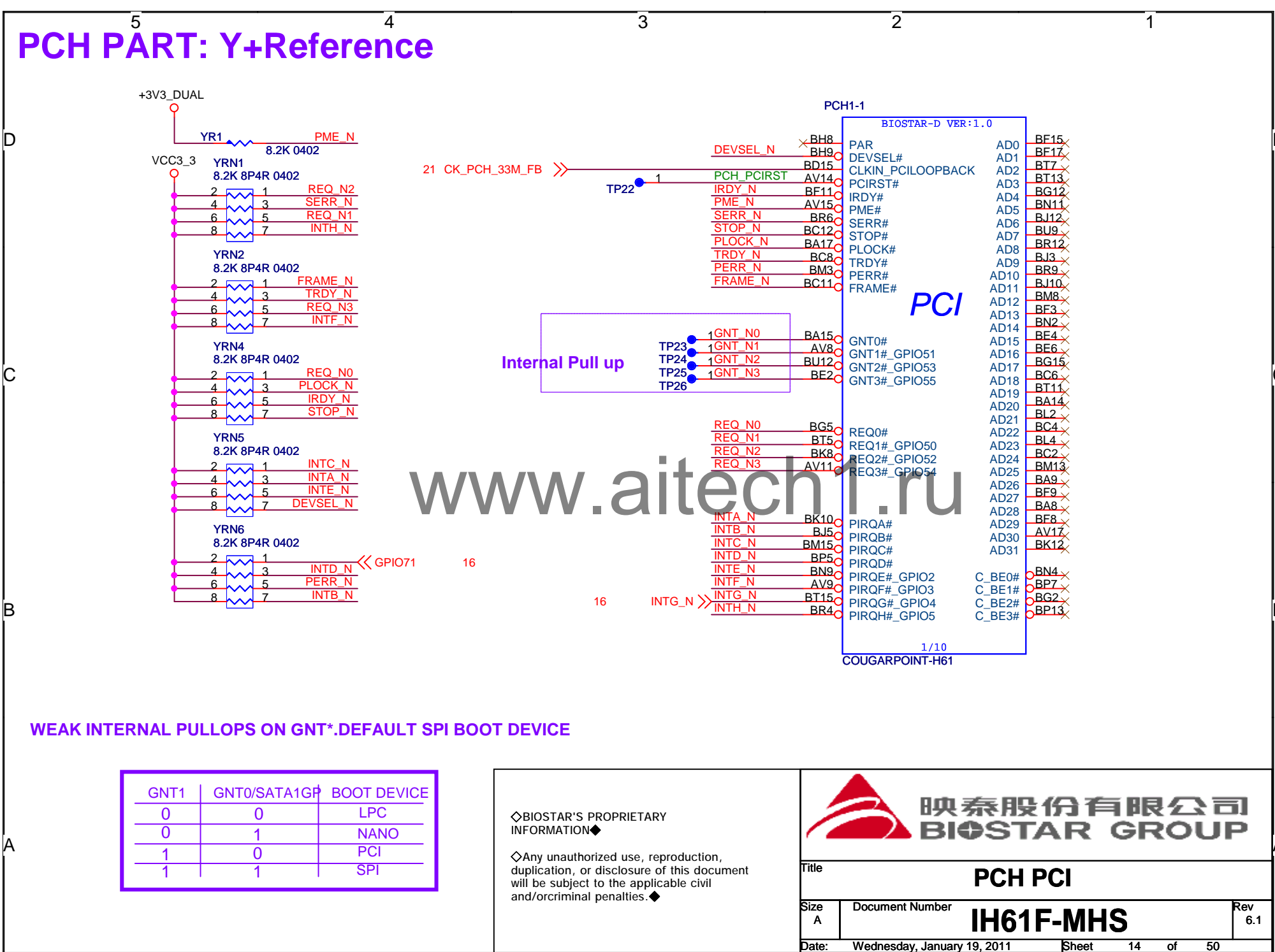
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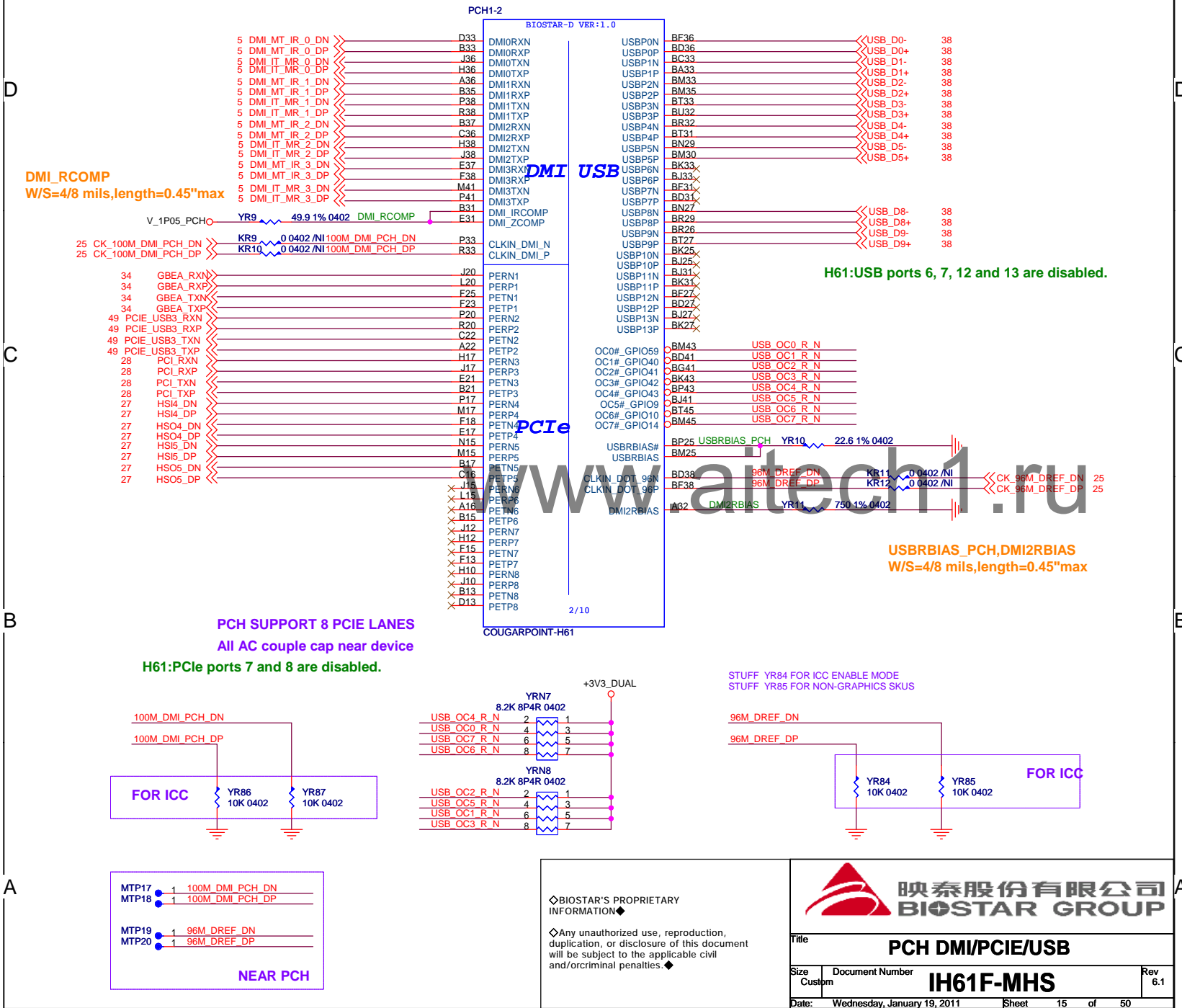
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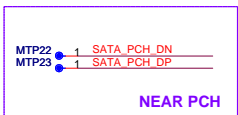
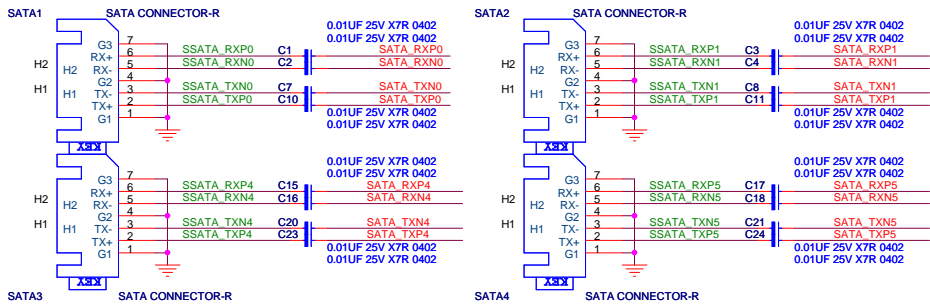
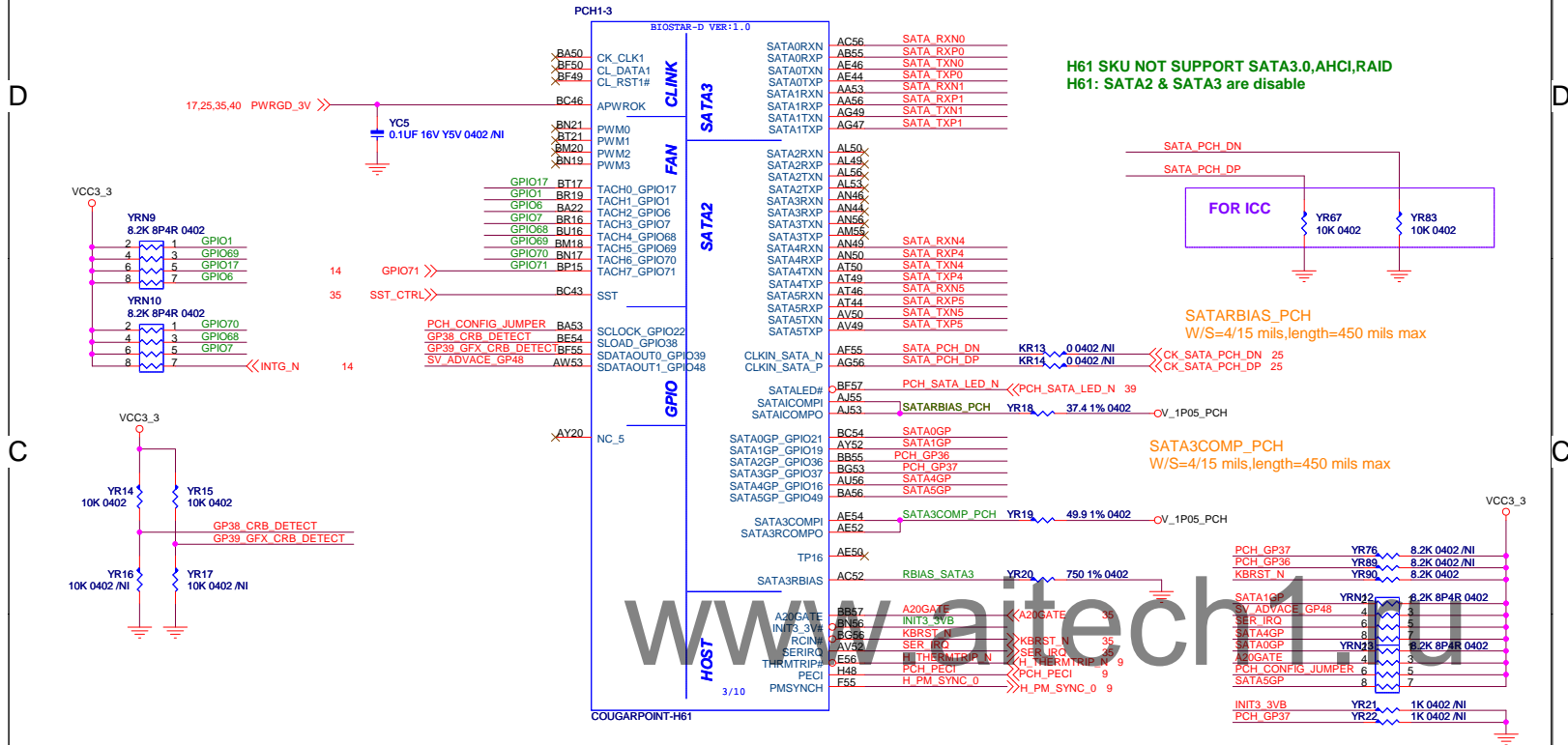
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# PCH PART: Y+Reference



Title			PCH DMI/PCIE/USB
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## PCH PART: Y+Reference



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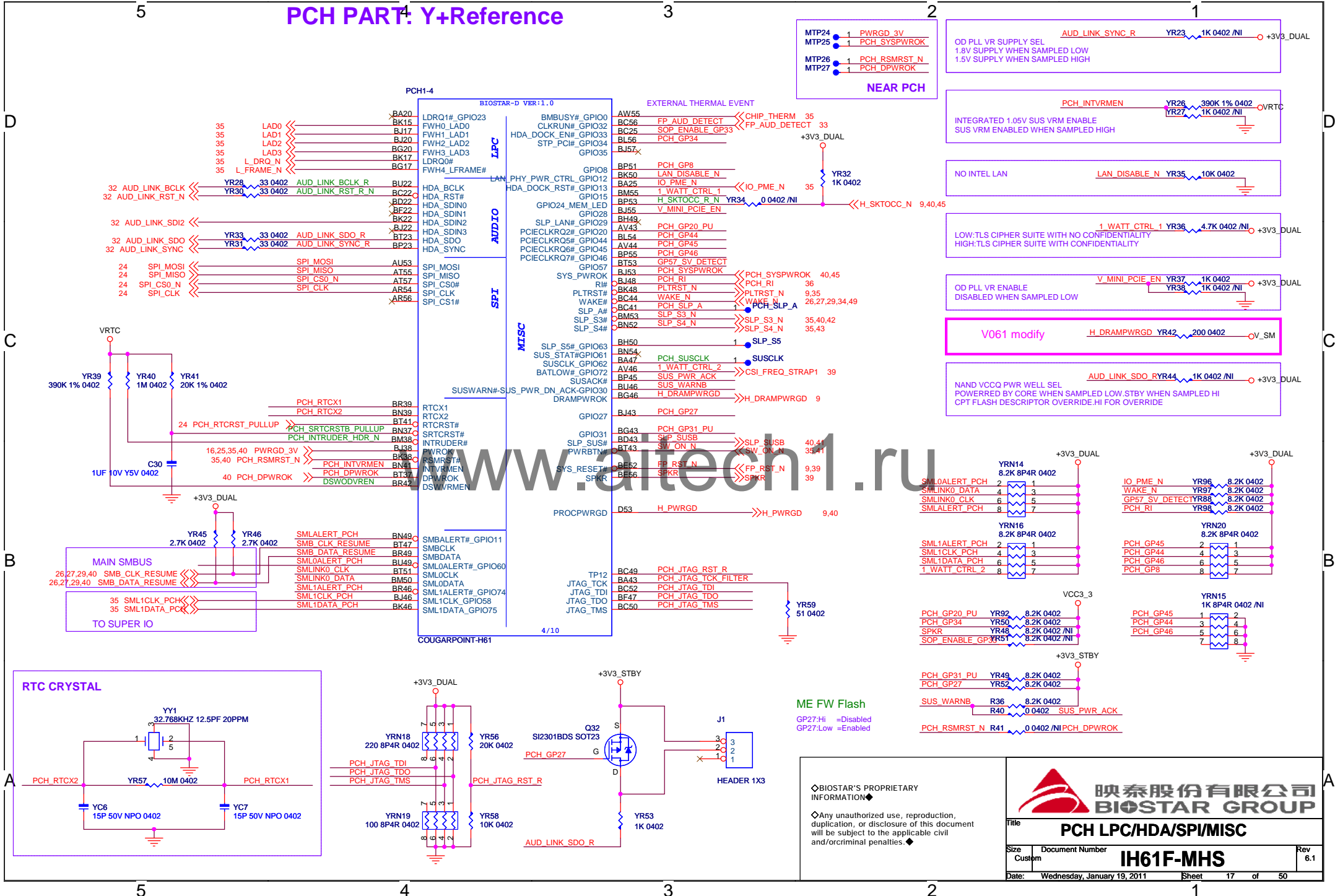


Title	PCH CLINK/SATA/CPU HOST
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Custom		

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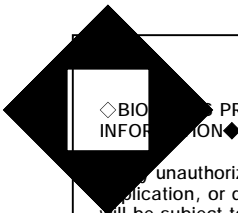
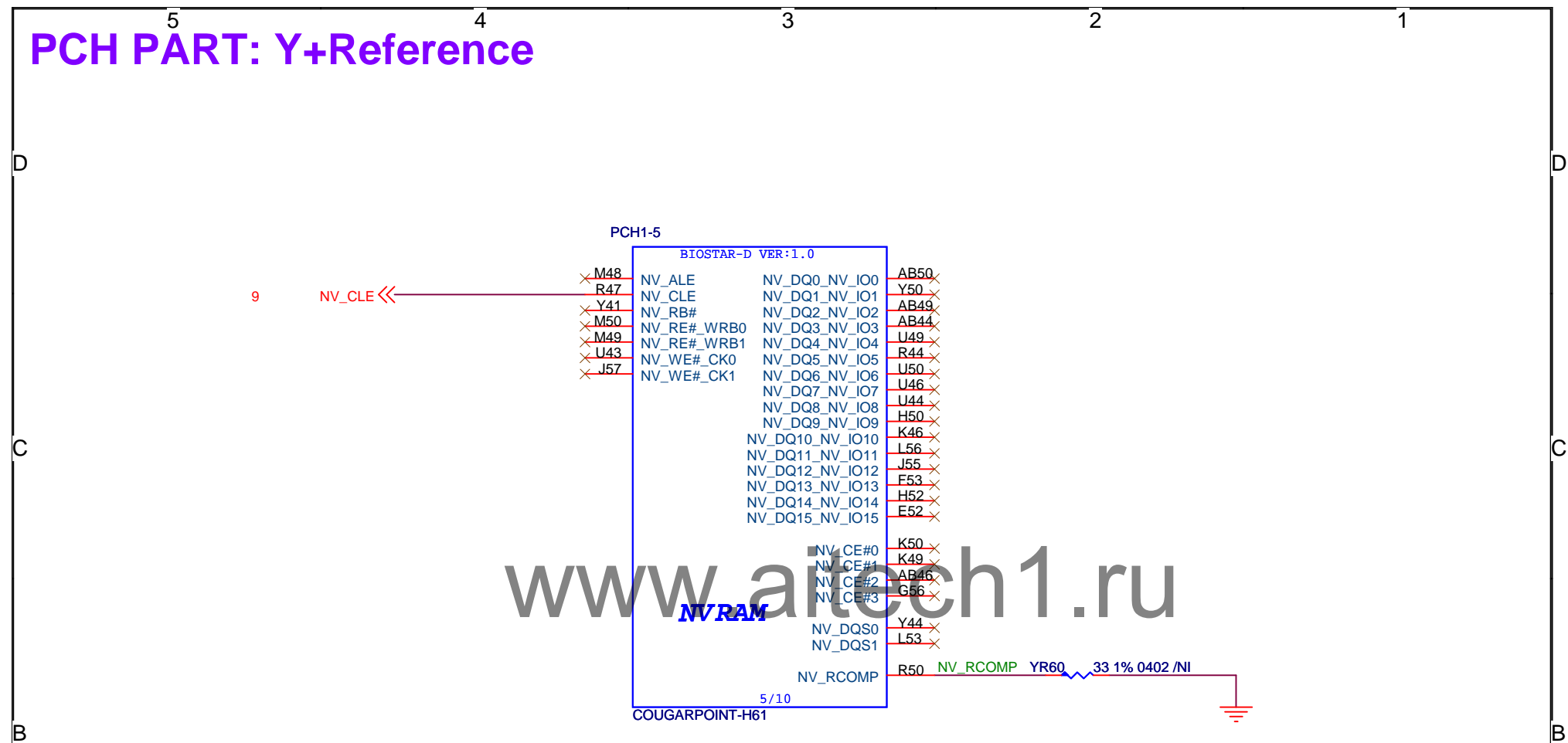
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Title: **PCH LPC/HDA/SP/MISC**

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# PCH PART: Y+Reference



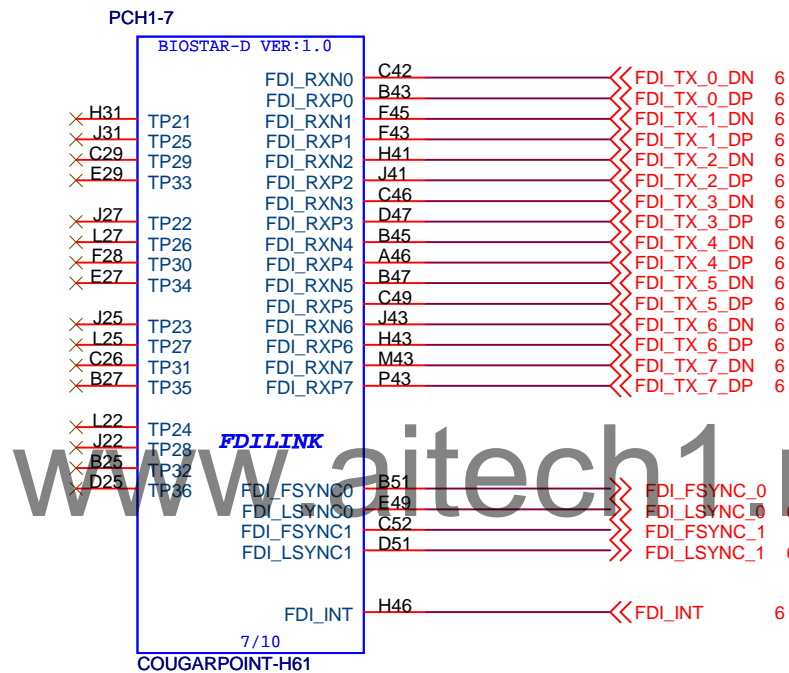
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Title <b>PCH NVRAM</b>		
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Title  
**PCH FDI LINK**

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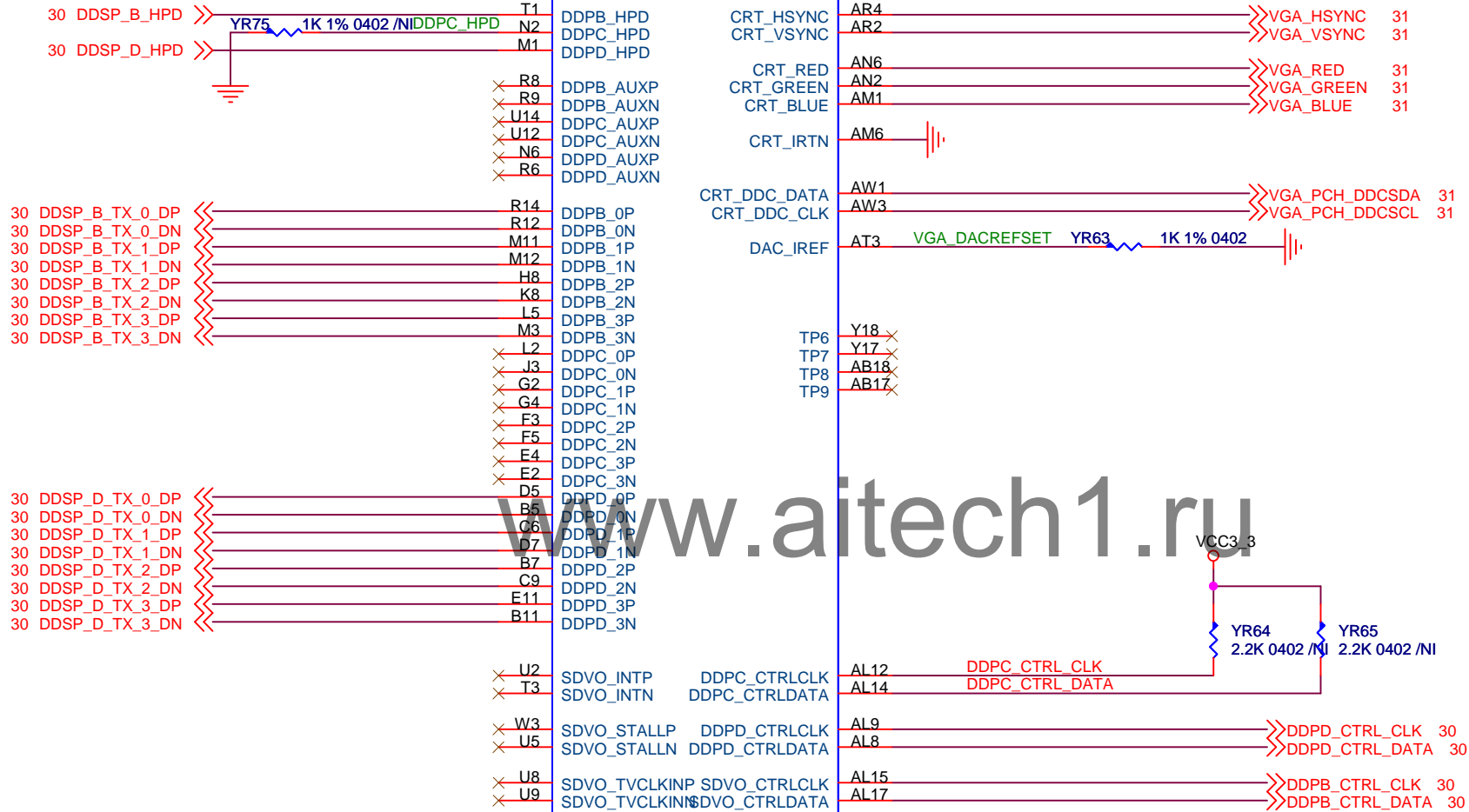


# PCH PART: Y+Reference

3.3V TOLERANT,HIGH ACTIVE  
V061 ADD

PCH1-6

BIOSTAR-D VER:1.0



REMOVE LEVEL SHIFTER WHEN TRACE LENGTH LESS THAN 9.25 INCHES

	FUNCTION
PORTB	DVI OR SDVO
PORTC	DISPLAY PORT
PORTD	HDMI/DVI/eDP

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Title **PCH VGA/DISPLAY PORT**

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**PCH PART: Y+Reference**

REF CRB

PCH1-8

BIOSTAR-D VER:1.0

35 PCLK\_IO << YR80 22 0402 PCH\_PCI0 AT11 CLKOUT\_PCH0 CLKIN\_GND1\_N R27 CK\_100M\_PCH\_IN\_DN

14 CK\_PCH\_33M\_FB << YR81 22 0402 PCH\_PCI1 AN14 CLKOUT\_PCH1 CLKIN\_GND1\_P P27 CK\_100M\_PCH\_IN\_DP

AT12 CLKOUT\_PCH2 CLKIN\_GND0\_N W53 CK\_CSI\_PCH\_IN\_DN

AT17 CLKOUT\_PCH3 CLKIN\_GND0\_P V52 CK\_CSI\_PCH\_IN\_DP

AT14 CLKOUT\_PCH4 CLKOUT\_ITPXPDP\_N R52

CLKOUT0 1 P\_CLKOUT0 AT9 CLKOUT\_PCH7N AE2 USB3\_CLKN 49

35 IO\_48MHZ << YR82 22 0402 PCH\_CKO BA5 CLKOUT\_PCH7P AF1 USB3\_CLKP 49

V\_1P05\_PCH YR66 90.9 1% 0402 XCLK\_RCOMP AL2 CLKOUT\_FLEX0\_GPIO64 CLKOUT\_DMI\_N P31 CK\_PE\_100M\_MCP\_DN 9

25 CK\_14M\_PCH >> YR91 0 0402 /NI 14M\_PCH AN8 CLKOUT\_FLEX1\_GPIO65 CLKOUT\_DMI\_P R31 CK\_PE\_100M\_MCP\_DP 9

XTAL\_25M\_PCH\_OUT AJ5 XTAL25\_OUT N56

XTAL\_25M\_PCH\_IN AJ3 XTAL25\_IN M55

YR68 1M 0402 XTAL\_25M\_PCH\_IN YY2 25MHZ 20PF 30PPM

YC8 22P 50V NPO 0402 YC9 22P 50V NPO 0402

Match with PCIECLKRQ#

For CPU PCIE clock

FOR IC6

CK\_100M\_PCH\_IN\_DN YR69 10K 0402

CK\_100M\_PCH\_IN\_DP YR70 10K 0402

CK\_CSI\_PCH\_IN\_DN YR71 10K 0402

CK\_CSI\_PCH\_IN\_DP YR72 10K 0402

14M\_PCH YR73 10K 0402

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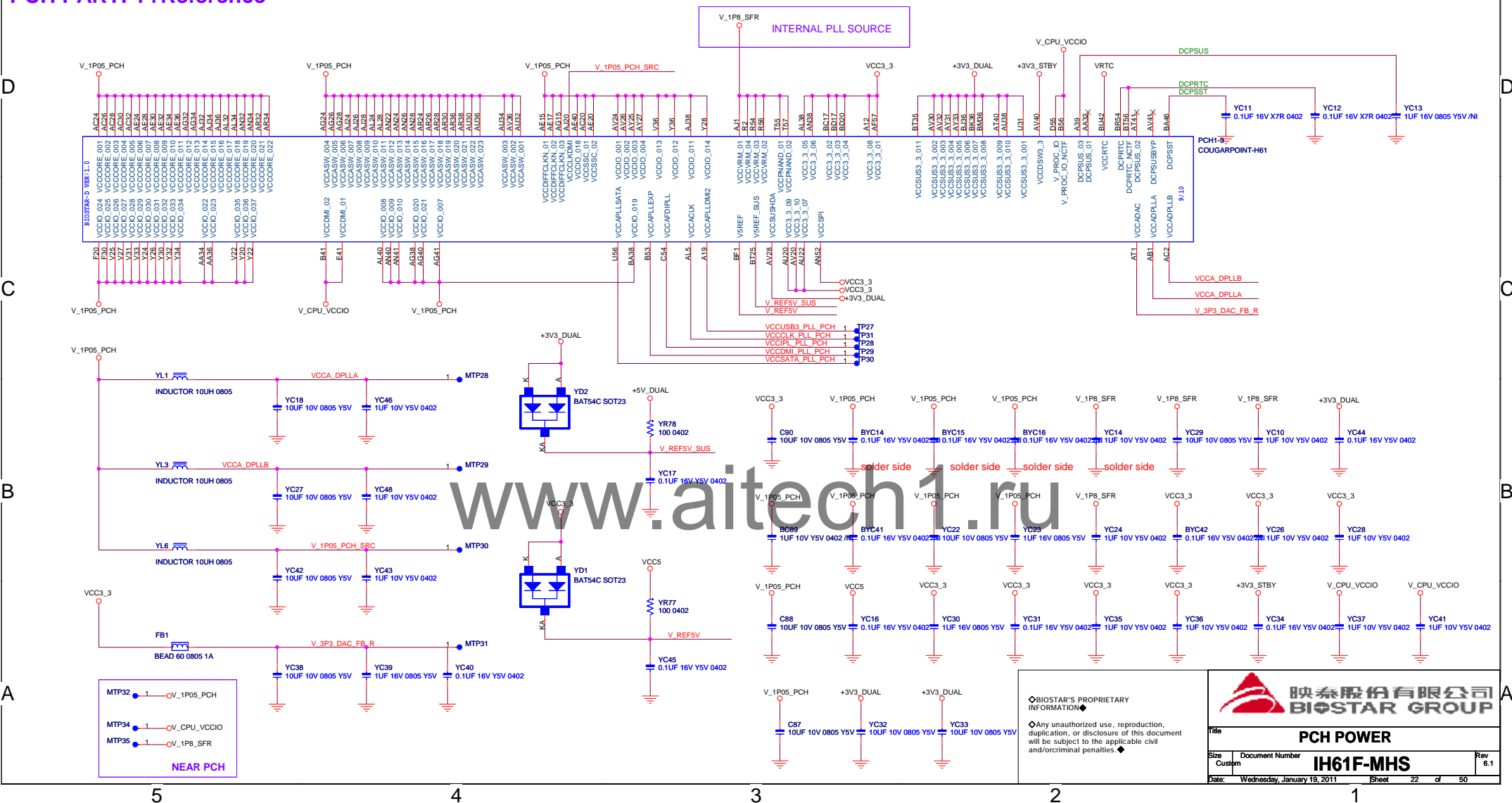
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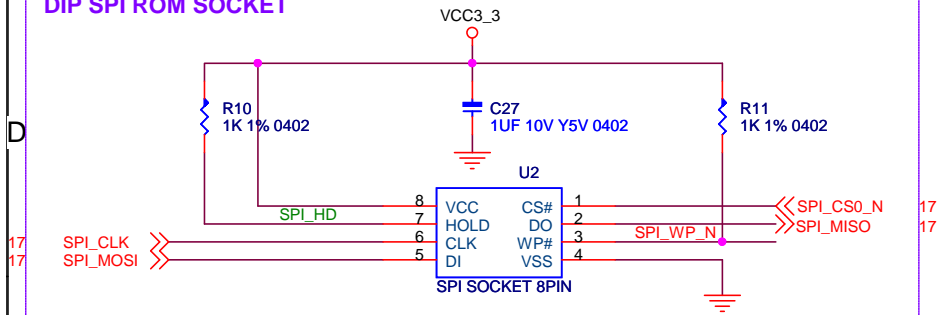
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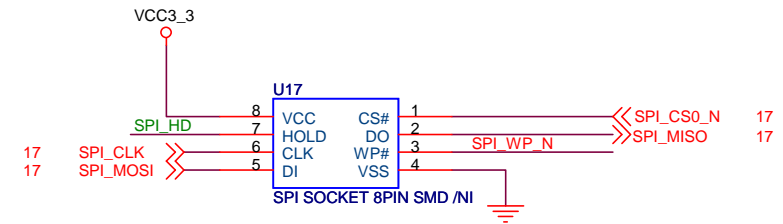




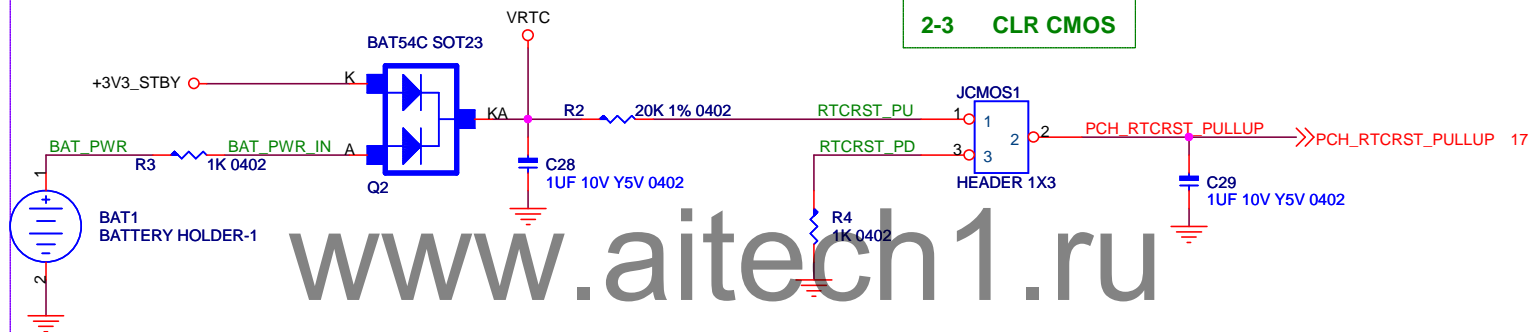
## DIP SPI ROM SOCKET



## SMD ROM SOCKET

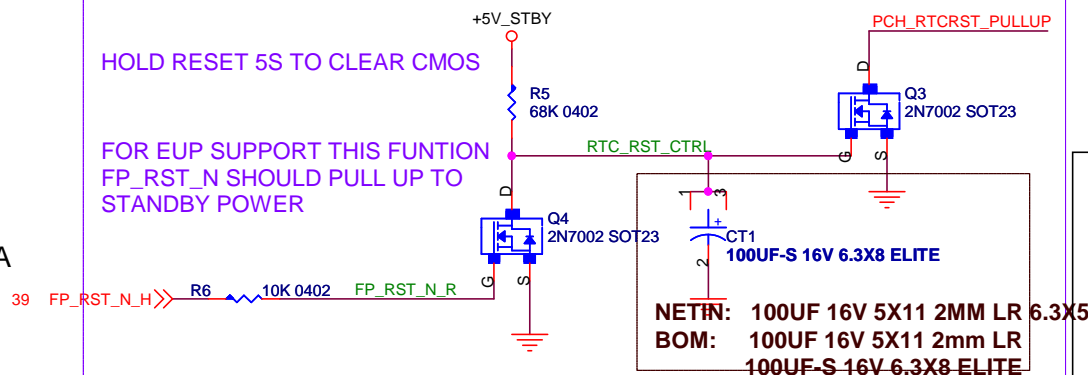


JCMOS  
1-2 NORMAL  
2-3 CLR CMOS



HOLD RESET 5S TO CLEAR CMOS

FOR EUP SUPPORT THIS FUNTION  
FP\_RST\_N SHOULD PULL UP TO  
STANDBY POWER



NETIN: 100UF 16V 5X11 2MM LR 6.3X5  
BOM: 100UF 16V 5X11 2mm LR  
100UF-S 16V 6.3X8 ELITE

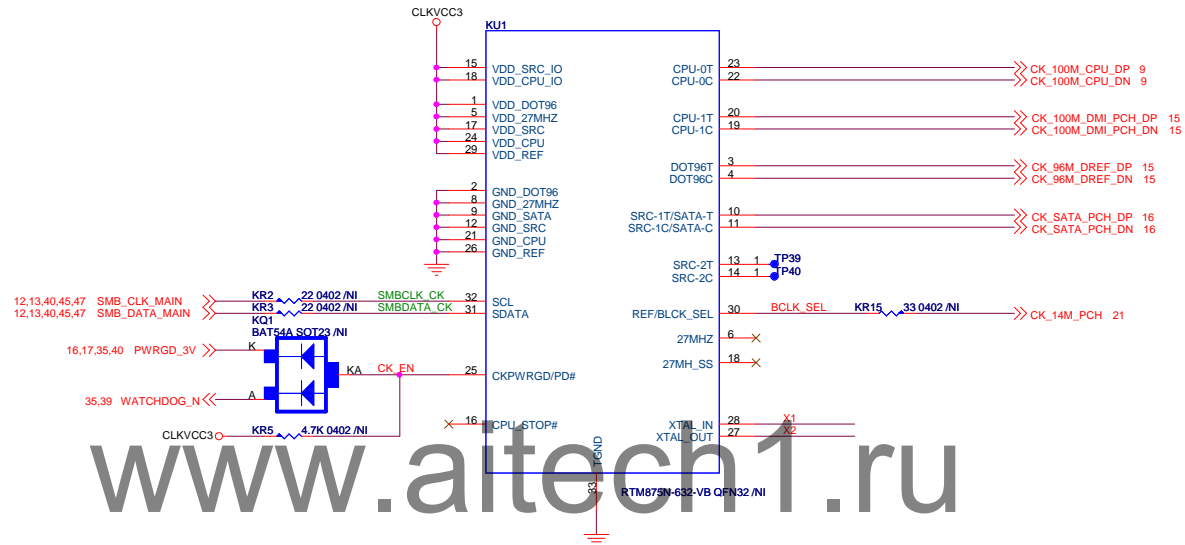
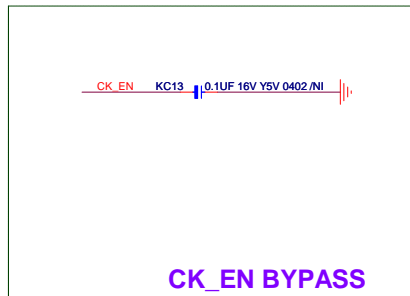
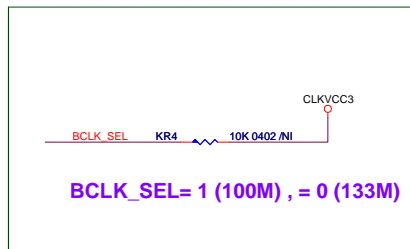
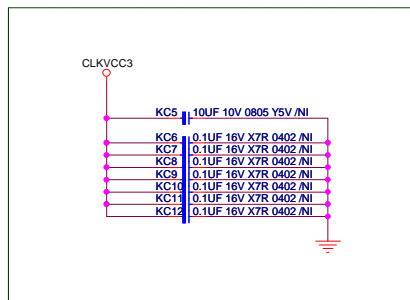
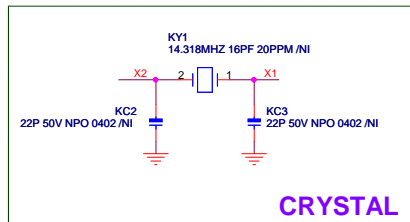
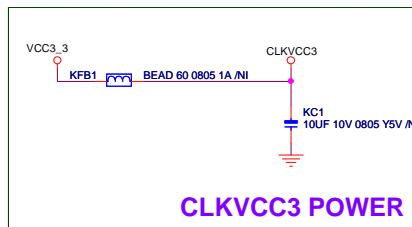
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Title			
SPI ROM/RTC CRYSTAL/BAT			
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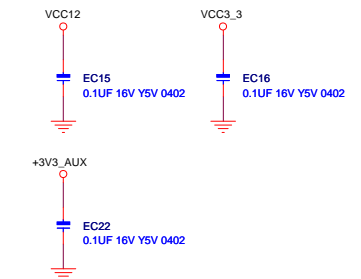
# CLOCK GEN PART: K+Reference



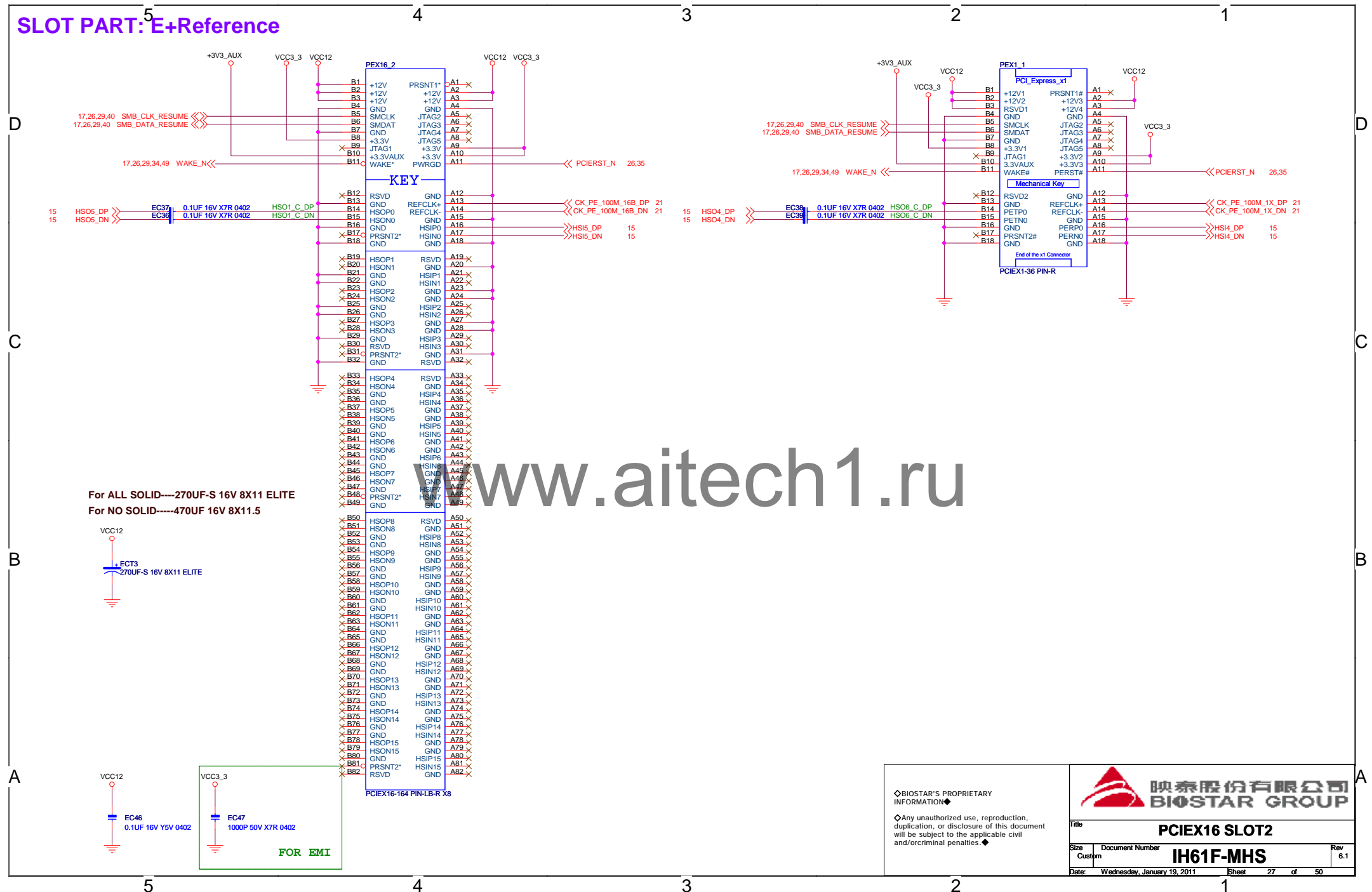
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<b>Title CK505 CLOCK GENERATOR</b>	
Size	Document Number
Custom	<b>IH61F-MHS</b>
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## 1



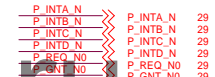
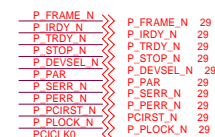
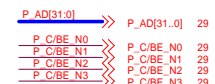
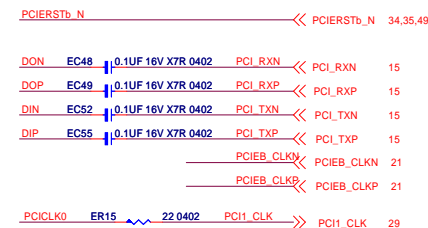
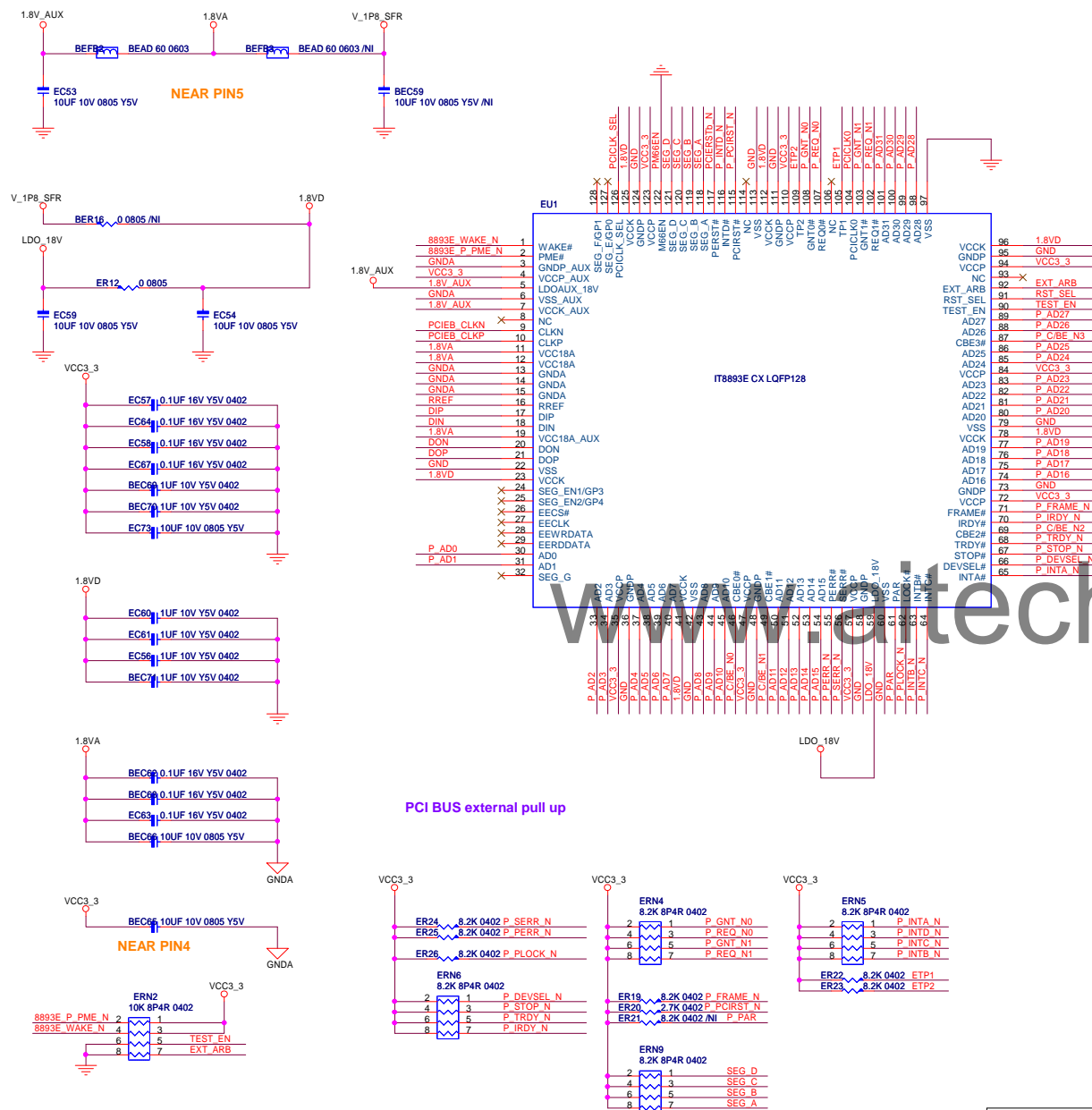
# SLOT PART: E+Reference



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<p><b>Title</b> <b>PCIEX16 SLOT2</b></p>			
Size	Document Number	Rev	
Custom	<b>IH61F-MHS</b>	6.1	
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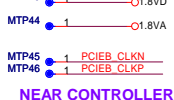
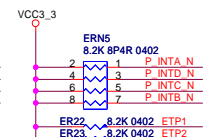
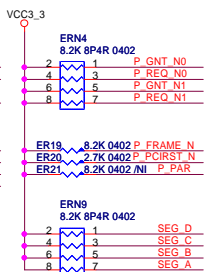
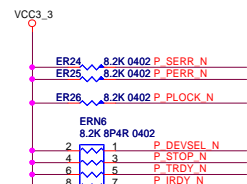
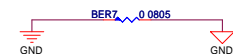
## SLOT PART: E+Reference



M66EN = LOW : DISABLED

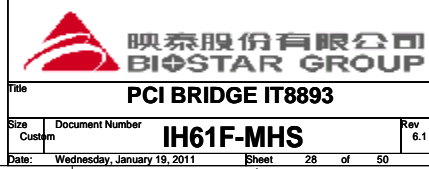


## Close to Chip



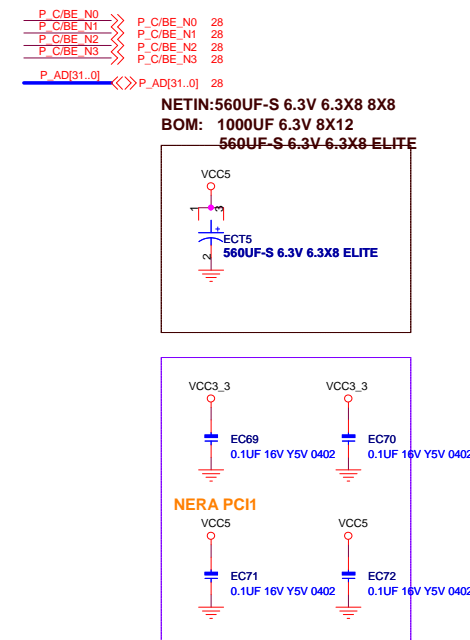
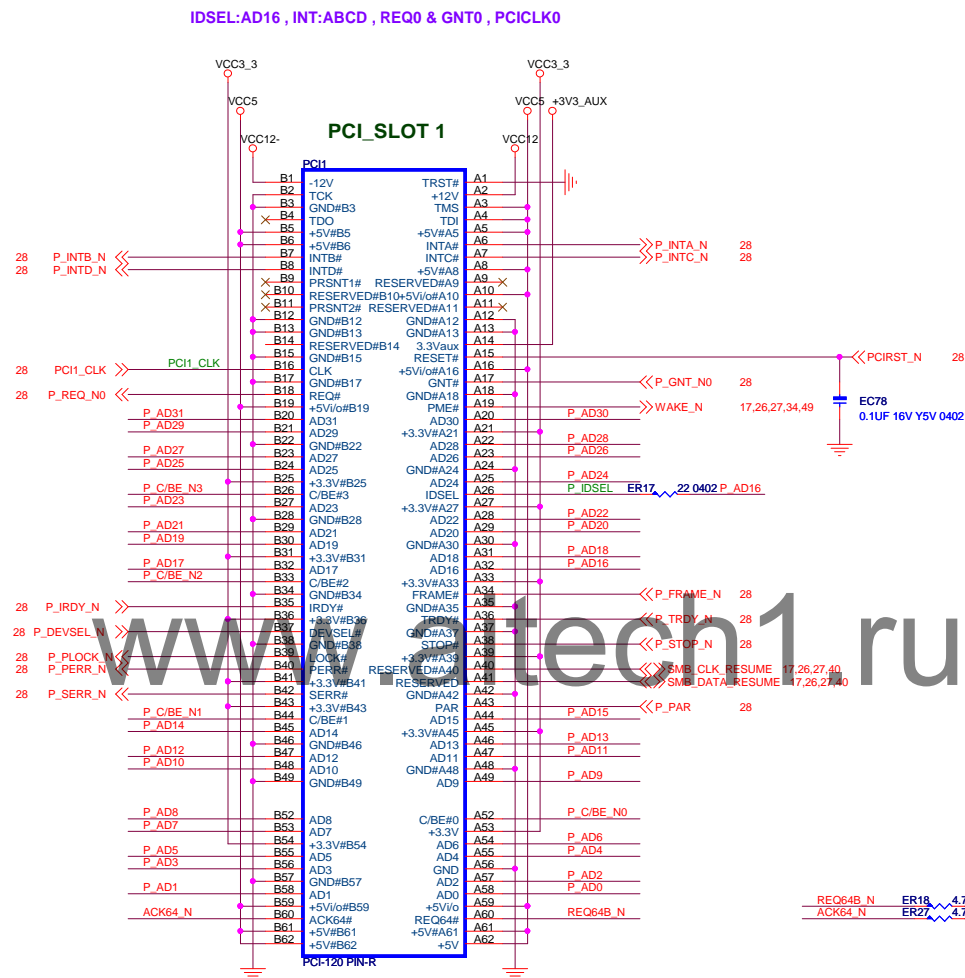
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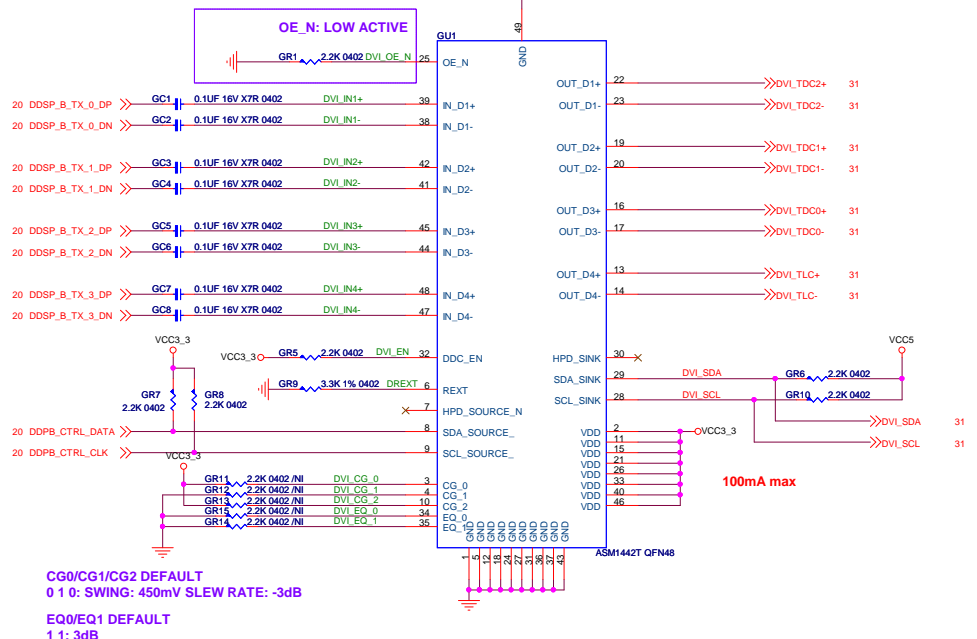
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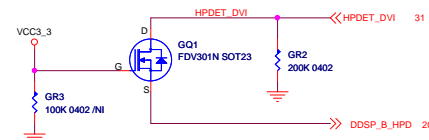
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Size	Document Number	<b>IH61F-MHS</b>	
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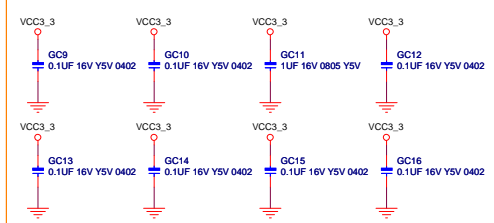
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For 1442T, RESERVE THIS CIRCUIT

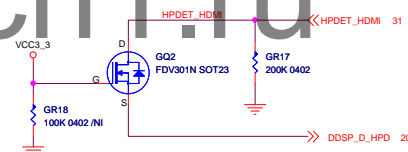


CLOSE TO GU1 VDD PIN

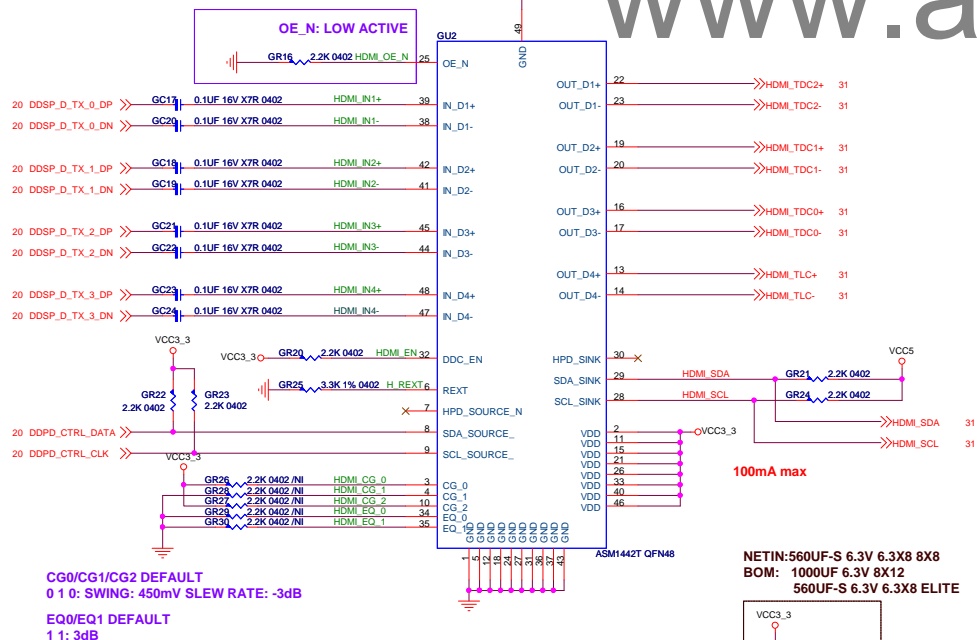
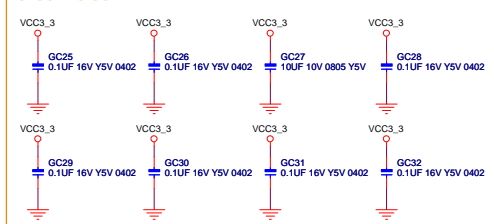


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For 1442T, RESERVE THIS CIRCUIT



CLOSE TO GU2 VDD PIN

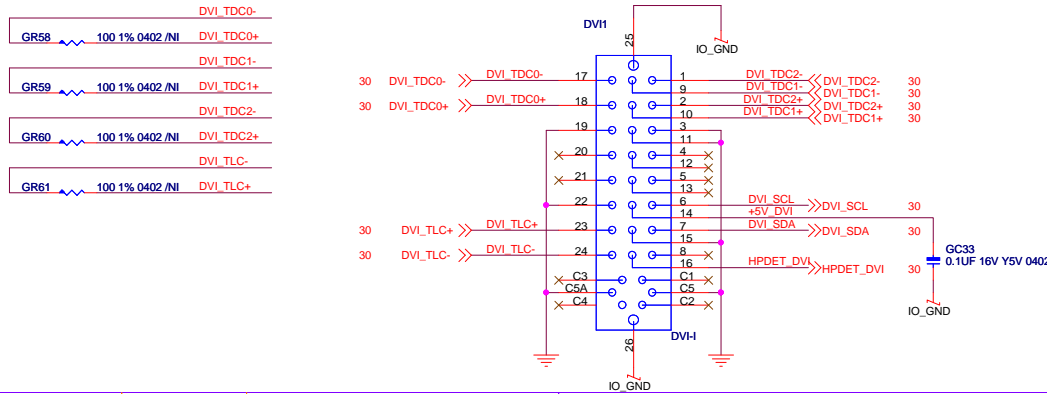


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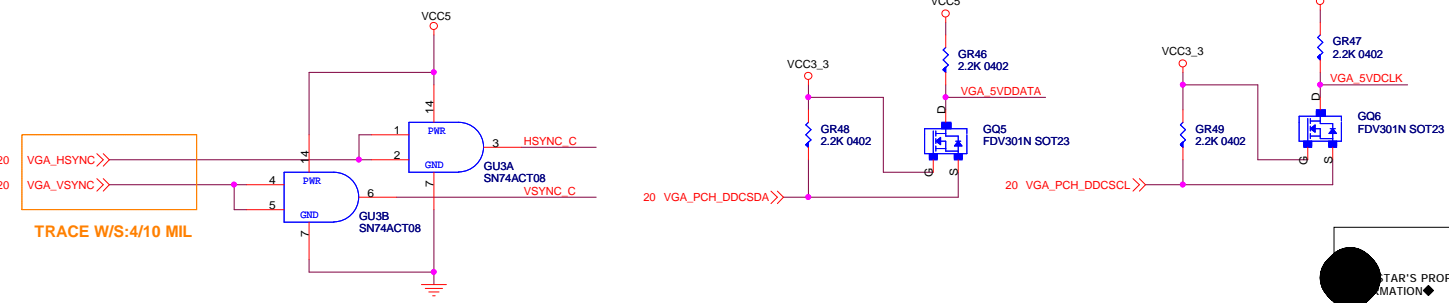
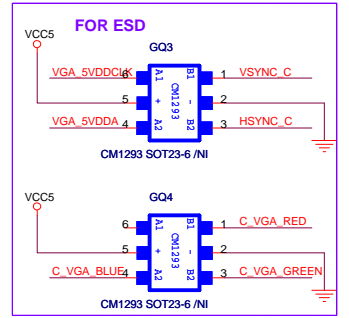
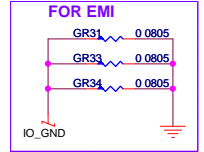
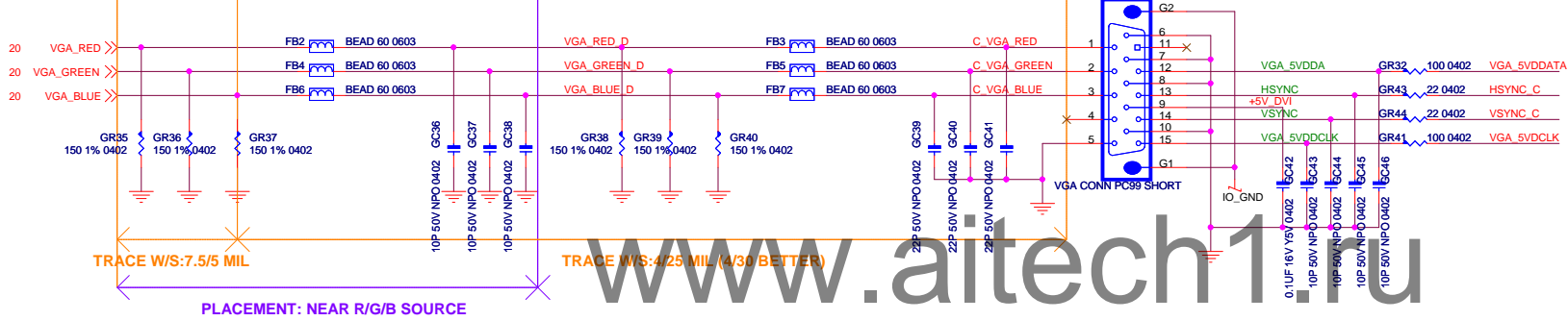
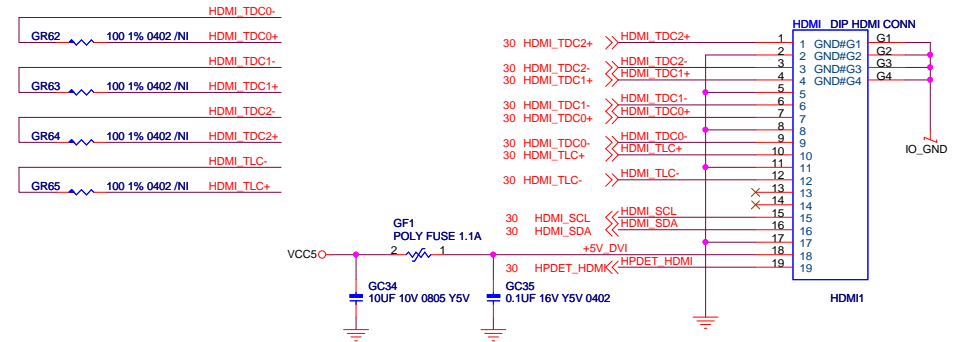
 <b>映泰股份有限公司</b> <b>BIOSTAR GROUP</b>		
Title <b>ASM1442T LEVEL SHIFTER</b>		
Size Custom	Document Number <b>IH61F-MHS</b>	Rev 6.1
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# GRAPHIC PART: G+Reference

## DVI CONNECTOR DVI CONNECTOR TYPE ACCORD WITH SPEC



## HDMI CONNECTOR



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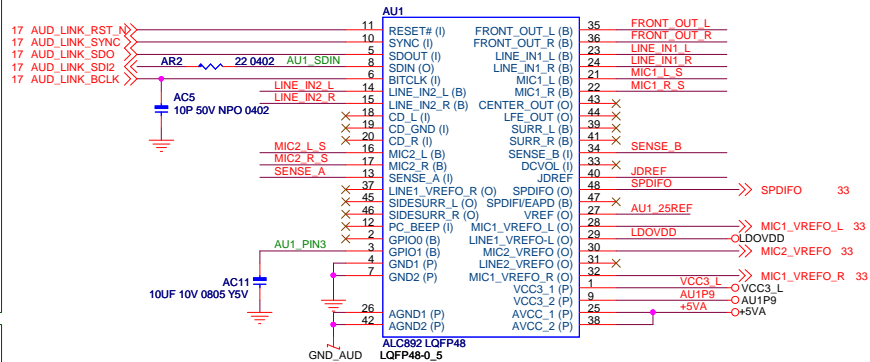
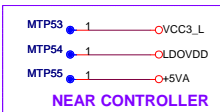
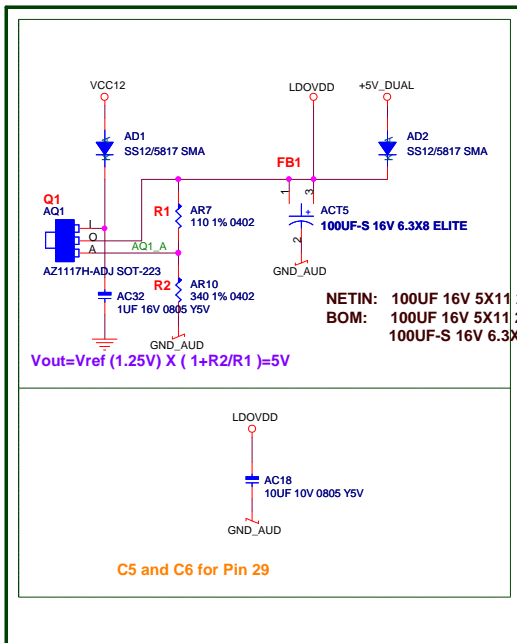
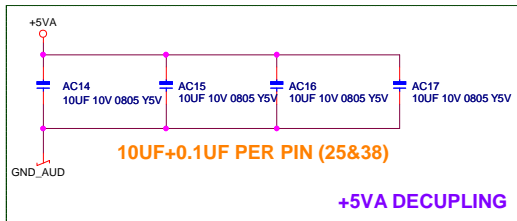
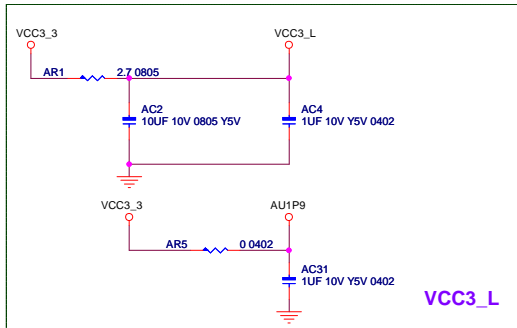
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**VGA/DVI/HDMI CONNECTOR**

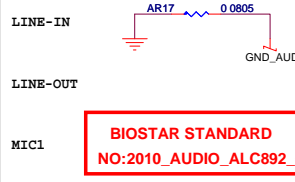
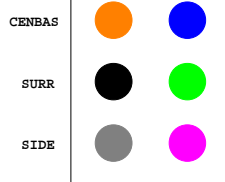
**IH61F-MHS**

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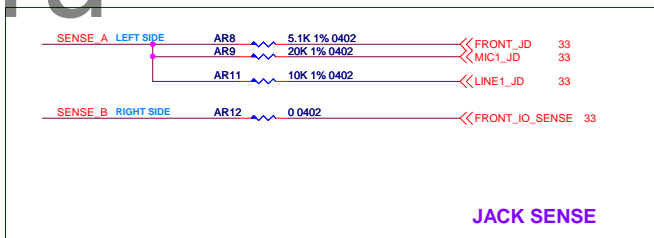
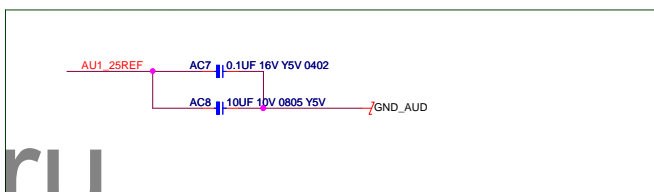
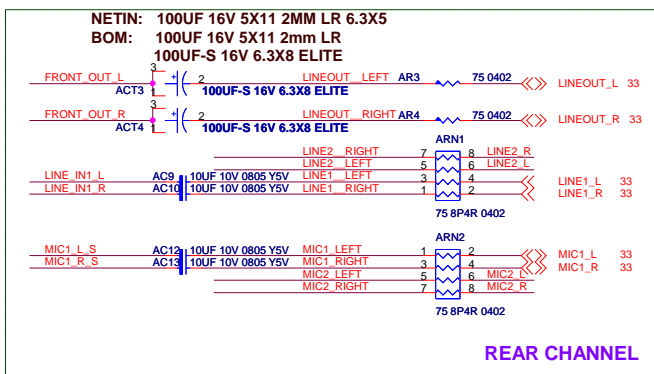
## AUDIO PART: A+Reference



## 7.1SPEAKER CONFIGURATION



BIOSTAR STANDARD  
NO:2010\_AUDIO\_ALC892\_01



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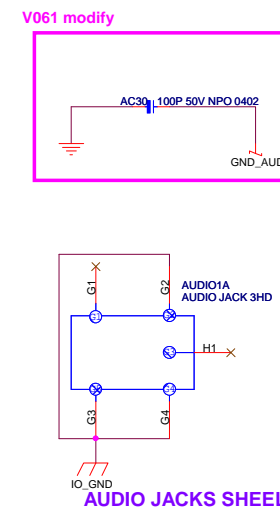
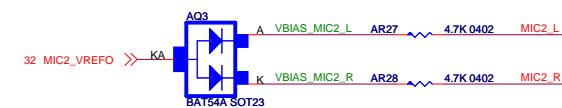
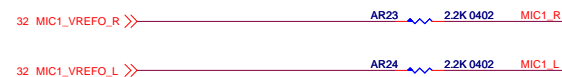
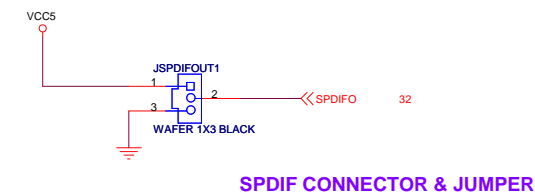
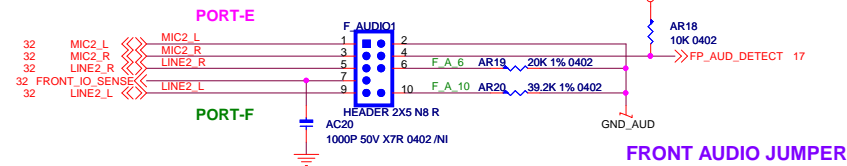
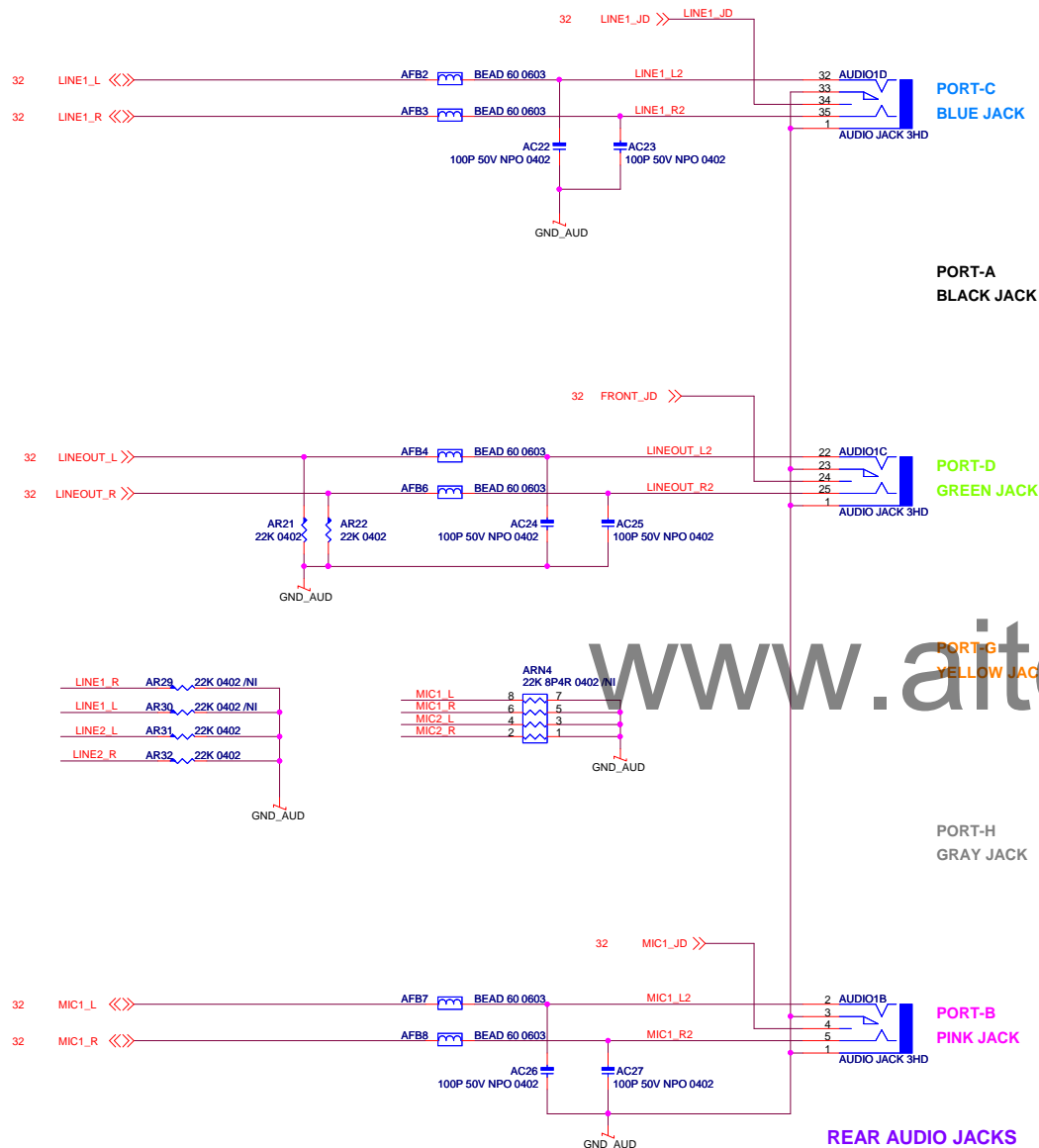
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Size Custom  
Document Number  
**IH61F-MHS**

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# AUDIO PART: A+Reference



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Title <b>AUDIO CONNECTOR</b>			
Size Custom	Document Number <b>IH61F-MHS</b>		Rev 6.1
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### LAN PART: L+Reference

**VDD33**

FOR RTL8111E INSTALL C1  
FOR RTL8105E NI C1  
PUT C1 TO PIN 12

**AVDD33\_REG**

**EVDD10 & VDD10**

FOR RTL8111E INSTALL C2,C3,C4  
FOR RTL8105E NI C2,C3,C4  
PUT C2 TO PIN6 , C3 TO PIN9, C4 TO PIN41

**CRYSTAL**

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**RTL8111EL-GR QFN48**

**CLOSE TO LAN IC**

**NEAR CONTROLLER**

**LAN CONNECTOR**

FOR RTL8111E,INSTALL R3 TO 0ohm  
FOR RTL8105E, INSTALL R3 TO 0.01UF

FOR RTL8111E,INSTALL R2; NI R1  
FOR RTL8105E, INSTALL R1;NI R2

FOR RTL8111E,RJ45USB1 VALUE IS LANUSB\_GBMA  
FOR RTL8105E, RJ45USB1 VALUE IS RJ45USBA CONN

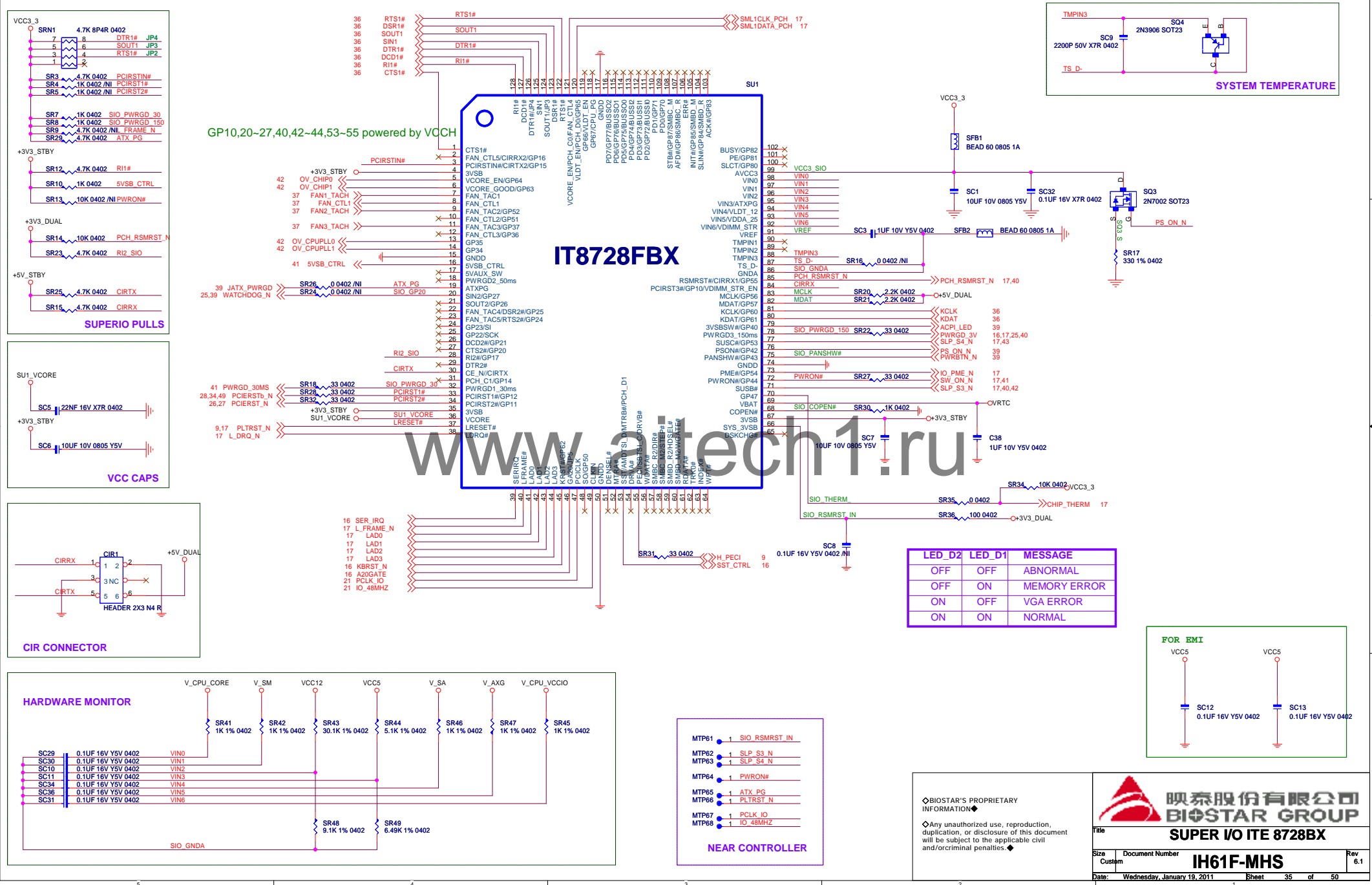
**LAN ESD**

**LAN STRAP AND PULLS**

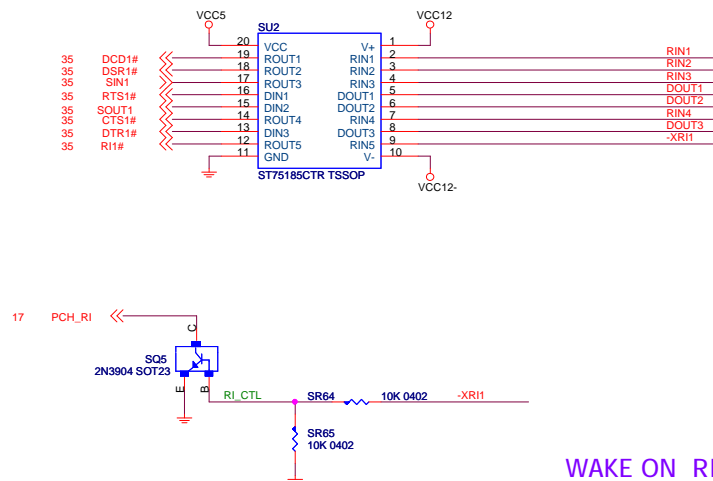
Internal EEPROM selected

COMPONENT CONTRAST LIST										
LAN PARTS	C1	C2	C3	C4		R1	R2	R3	RJ45 CONN	
RTL8111E	O	O	O	O		X	O	0ohm	LANUSB_GBMA	
RTL8105E	X	X	X	X		O	X	0.01uF	RJ45USBA CONN	

# SUPERIO PART: S+Reference

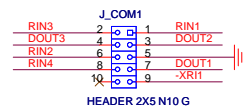


## AUDIO PART: A+Reference



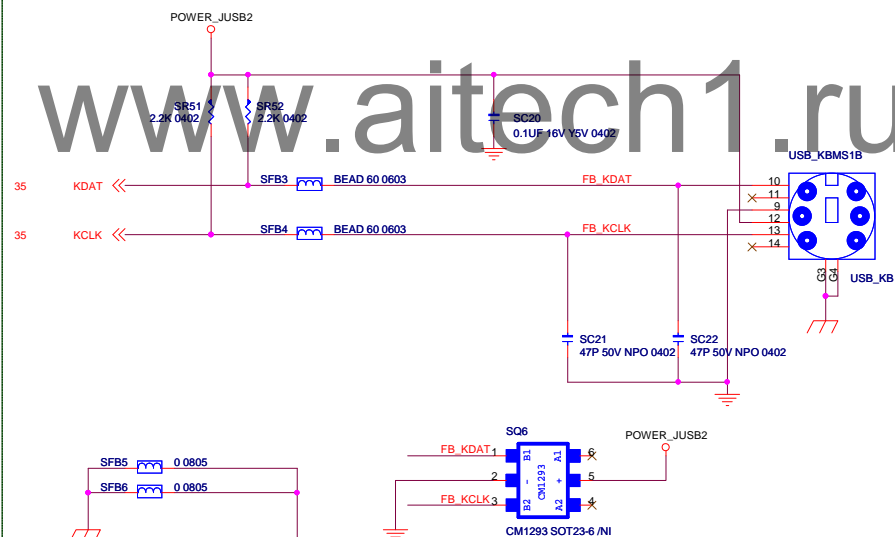
WAKE ON RING

OPTIONAL



COM PORT

FLOPPY



KEYBOARD & MOUSE

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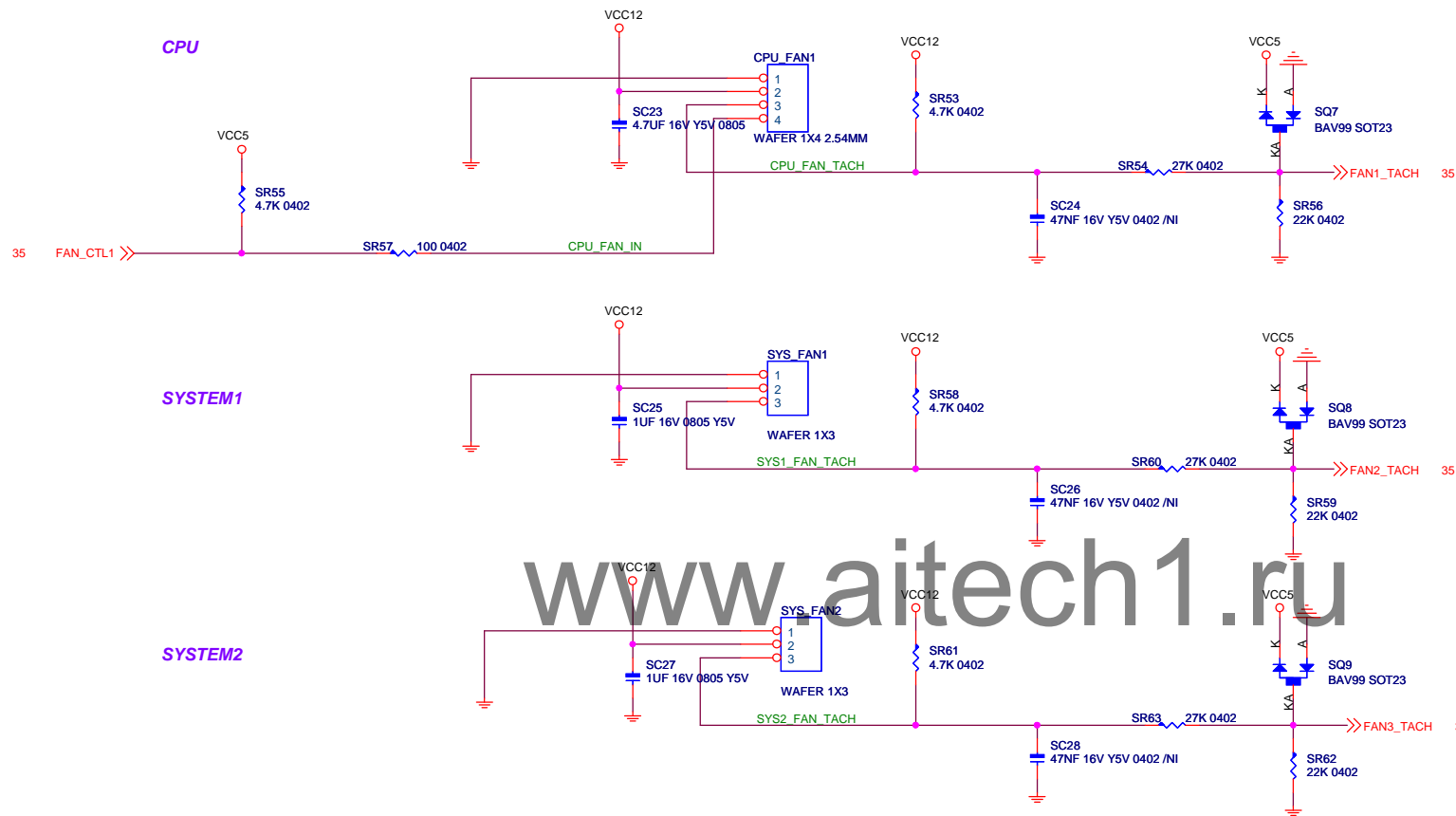


Title		
FDD / PS2 CONN		
Size	Document Number	Rev
Custom	IH61F-MHS	6.1
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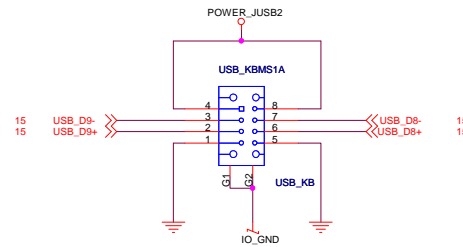
## AUDIO PART: A+Reference

### CPU FAN/SYSTEM FAN1/SYSTEM FAN2

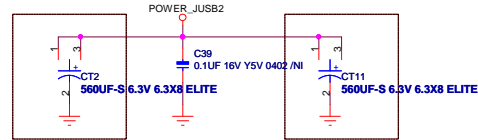
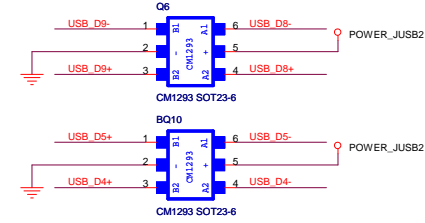
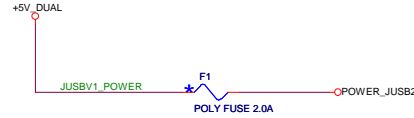


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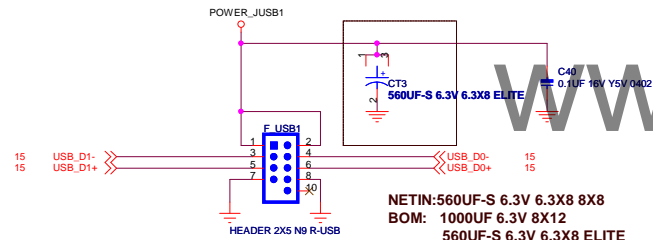
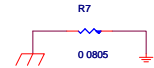
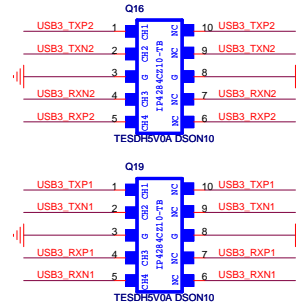
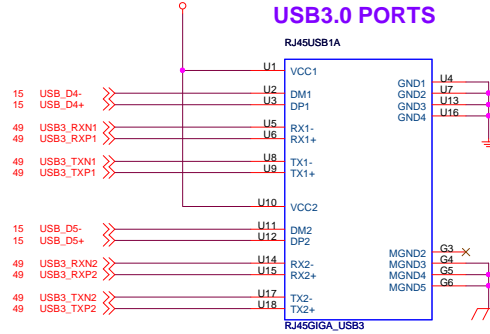
 <b>映泰股份有限公司</b> <b>BIOSTAR GROUP</b>		
Title <b>HW MONITOR/FAN CONTROL</b>		
Size Custom	Document Number <b>IH61F-MHS</b>	Rev 6.1
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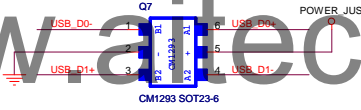
DEFAULT : 1-2 CLOSE



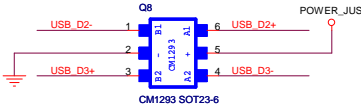
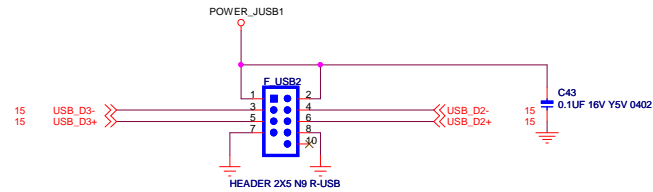
NETIN:560UF-S 6.3V 6.3X8 8X8  
BOM: 1000UF 6.3V 8X12  
560UF-S 6.3V 6.3X8 ELITE



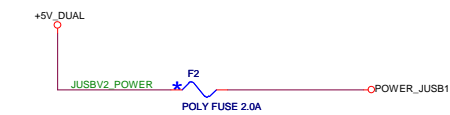
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560UF-S 6.3V 6.3X8 ELITE



FRONT PANEL USB



FRONT PANEL USB



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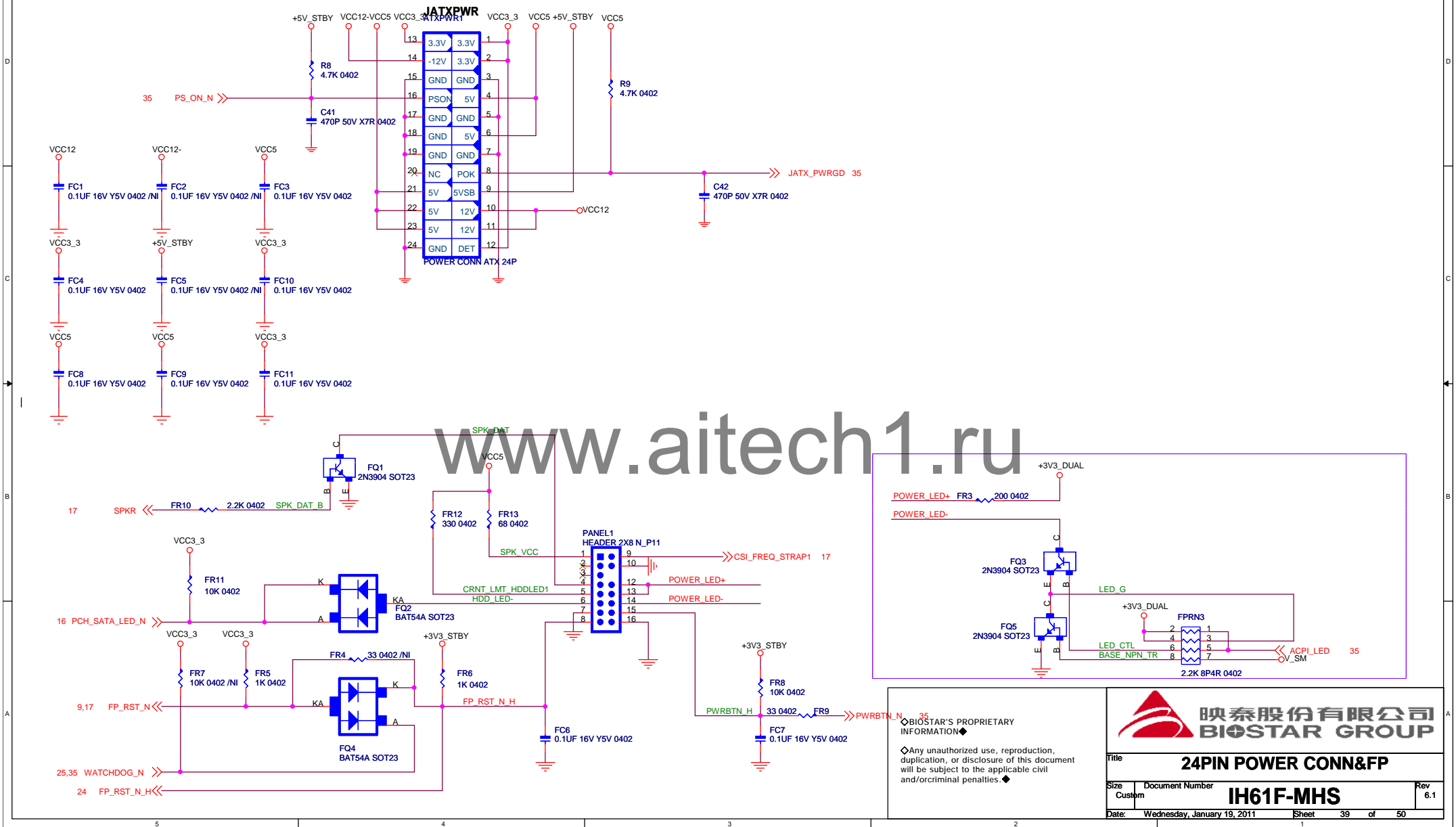
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**BIOSTAR GROUP**

Title: **USB CONN**

Size: Custom Document Number: **IH61F-MHS** Rev: 6.1

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# FP PART: F+Reference



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BIOSSTAR GROUP

**Title** 24PIN POWER CONN&FP

**Size** Custom

**Document Number** IH61F-MHS

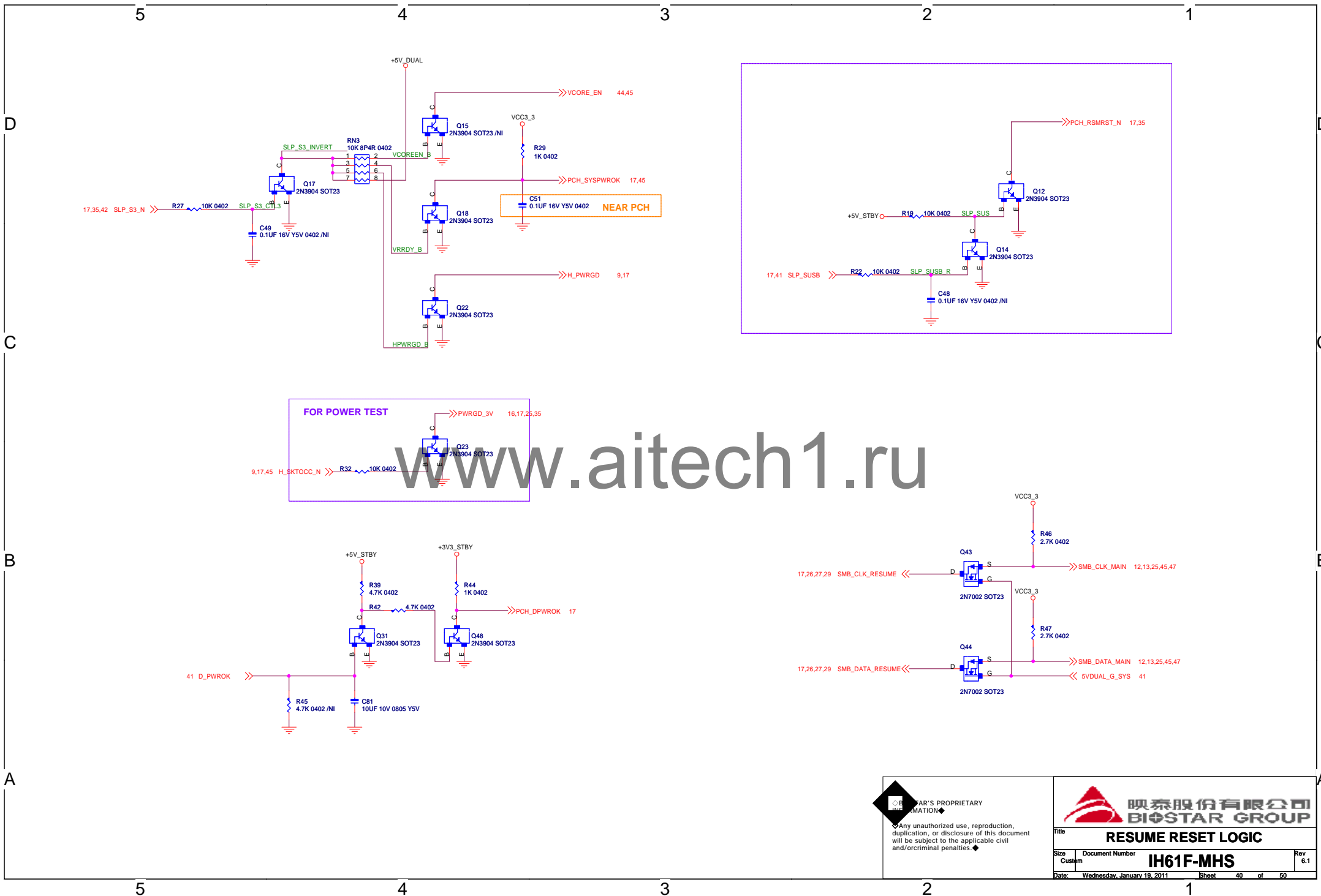
**Date:** Wednesday, January 19, 2011

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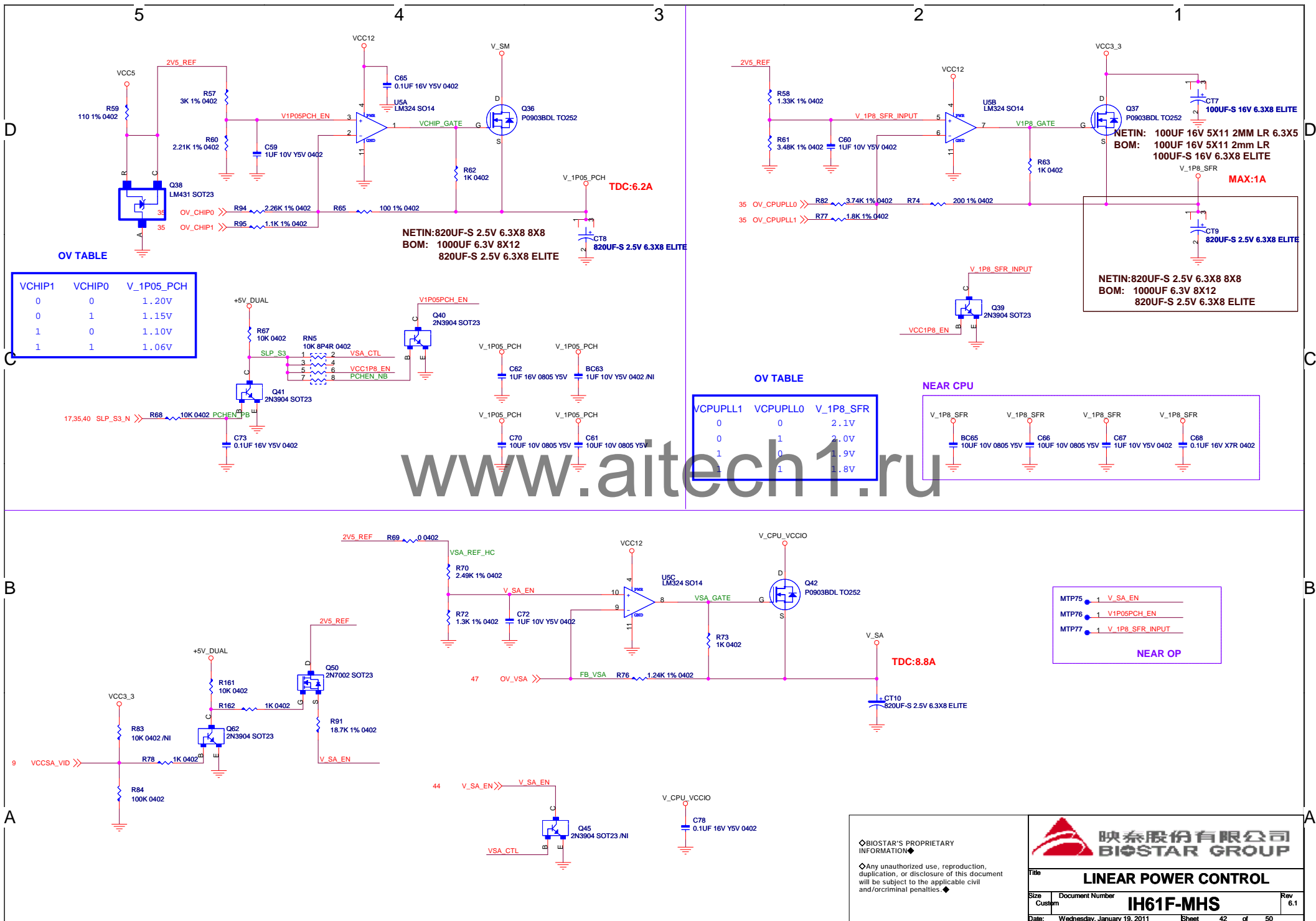


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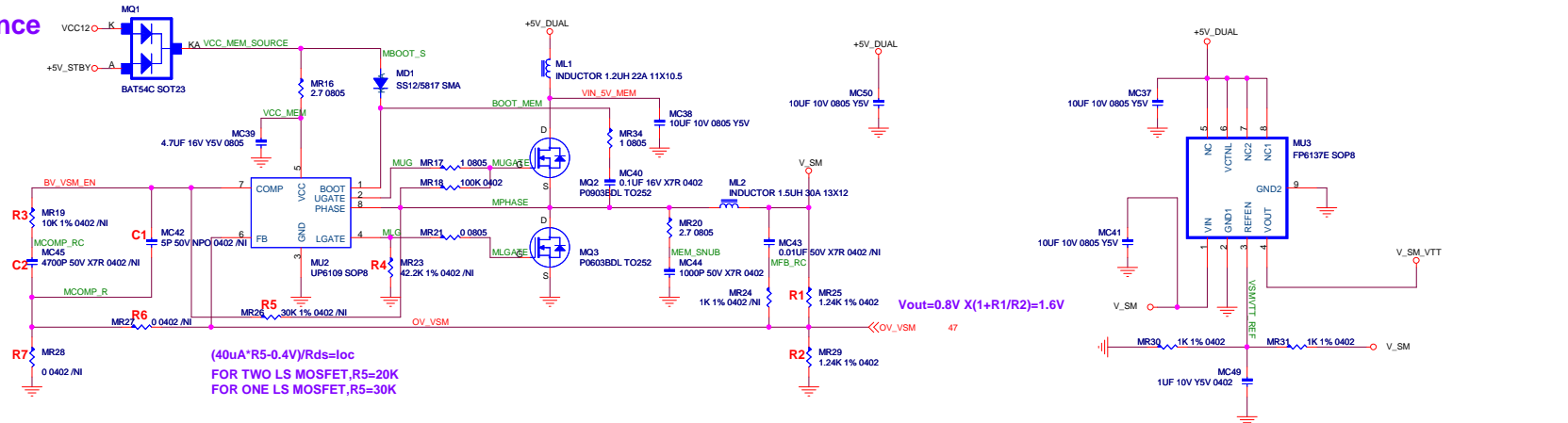
 <b>映泰股份有限公司</b> <b>BIOSAR GROUP</b>	
<b>RESUME RESET LOGIC</b>	
Title Size Custom	Document Number <b>IH61F-MHS</b>
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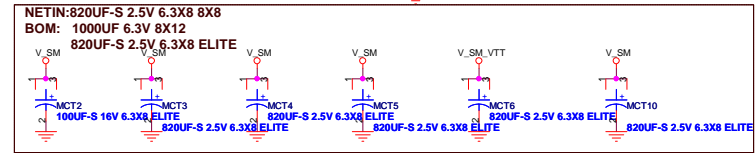
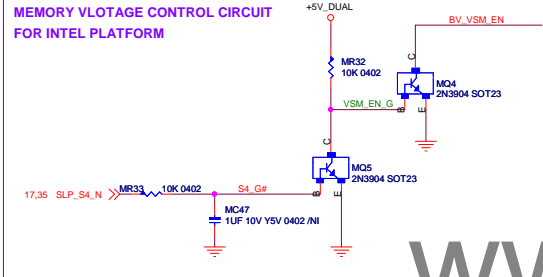


# MEMORY PART:M+Reference

	FP6321A	UP6101B	FP6327
R3	NI	13.7K 1% 0402	
R4	NI	26.1K 1% 0402	
R5	20K 0402	NI	
R6	NI	0 0402	
R7	NI	NI	
C1	NI	5P 50V NPO 0402	
C2	NI	4700P 50V X7R 0402	



## MEMORY VLOTAGE CONTROL CIRCUIT FOR INTEL PLATFORM



NETIN: 100UF 16V 5X11 2MM LR 6.3X5  
BOM: 100UF 16V 5X11 2mm LR  
100UF-S 16V 6.3X8 ELITE

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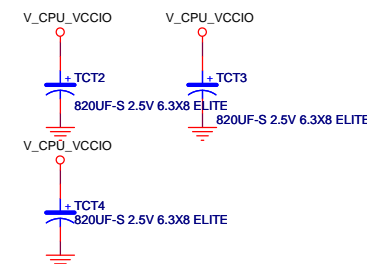
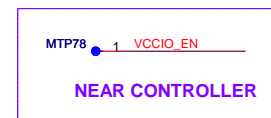
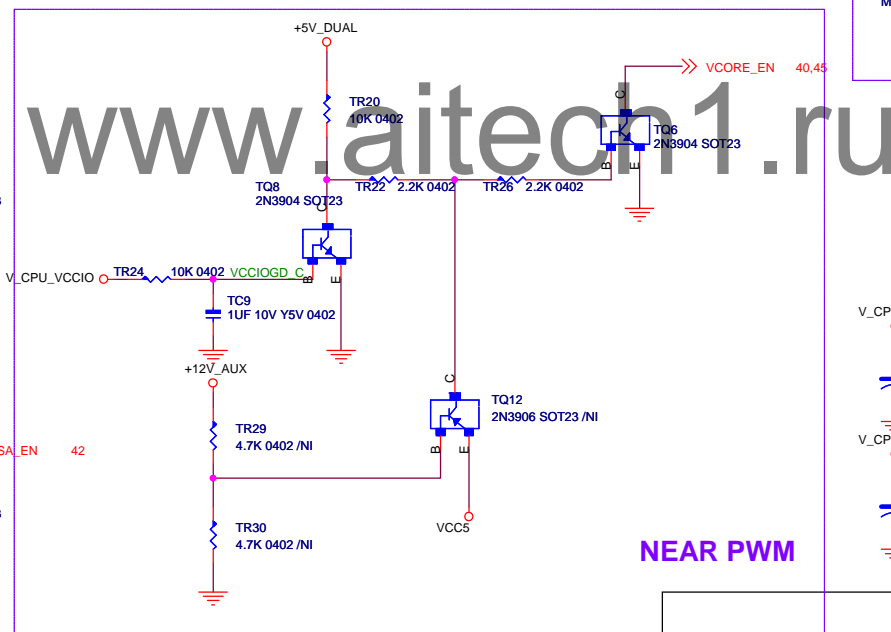
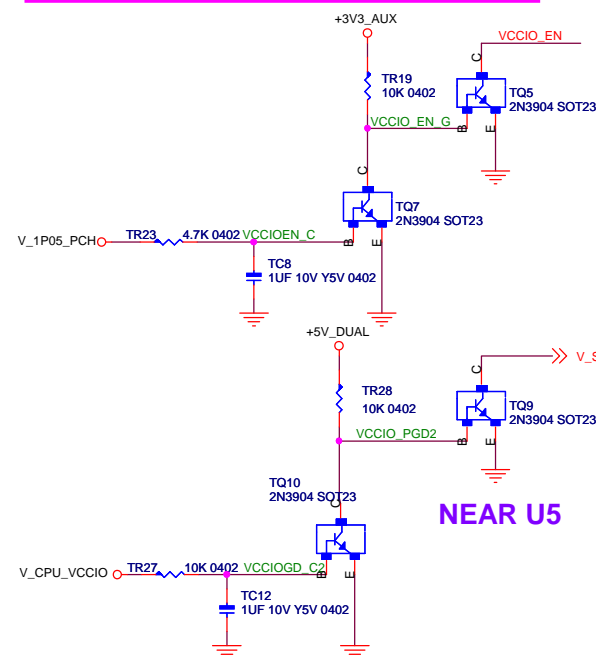
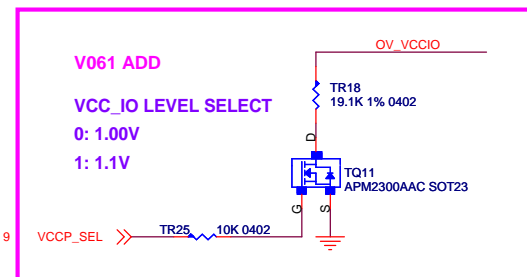
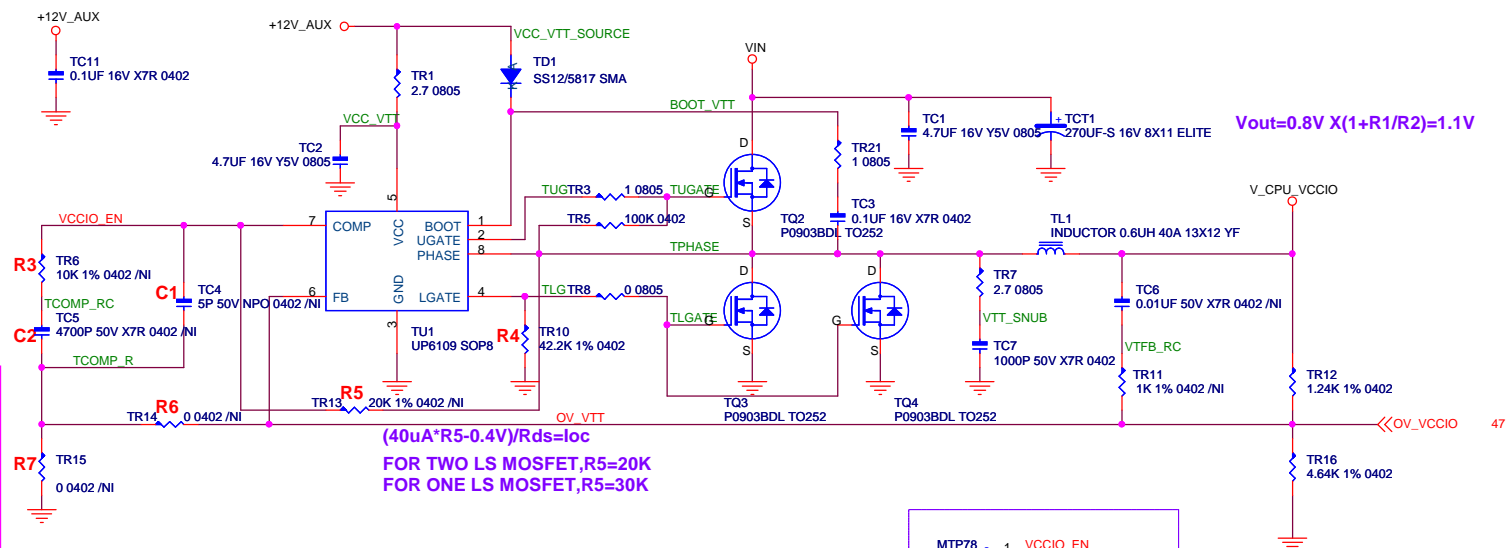
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# VTT POWER PART:T+Reference

	FP6321A	UP6101B	FP6327
R3	NI	13.7K 1% 0402	
R4	NI	26.1K 1% 0402	
R5	20K 0402	NI	
R6	NI	0 0402	
R7	NI	NI	
C1	NI	5P 50V NPO 0402	
C2	NI	4700P 50V X7R 0402	



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# CPU POWER PART:P+Reference

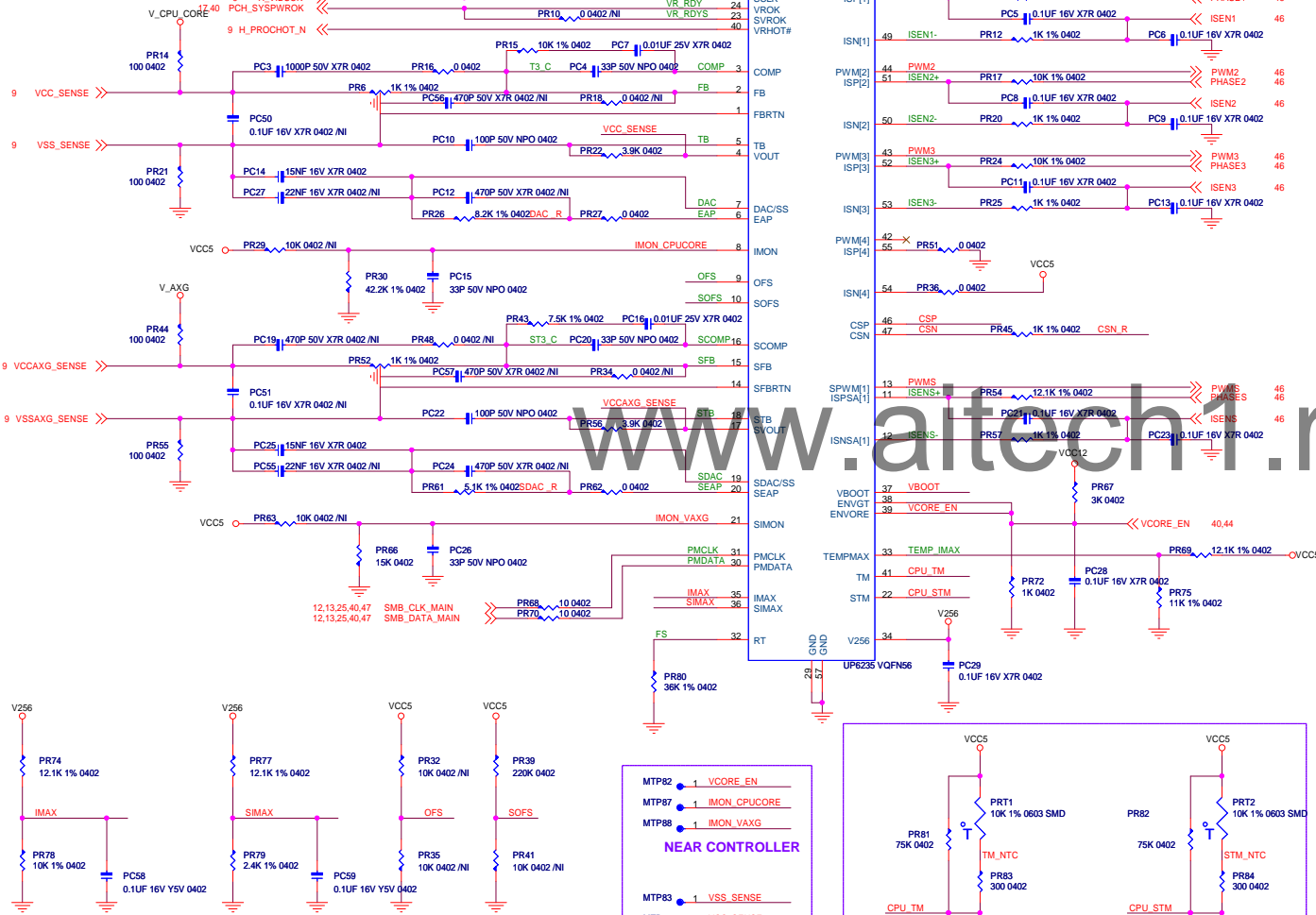
# VRD12: 3+1 HIGH1+LOW2

D/源供 CHOKE 0.6uH/40A/  
DCR0.8m/ELDA-1312-R60M-P/磁感...事

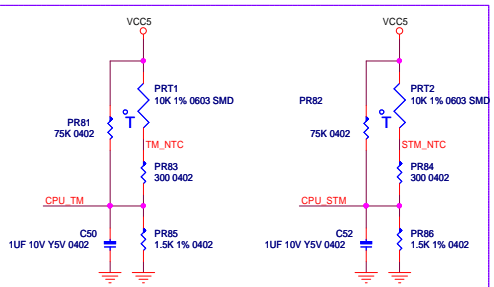
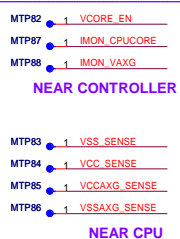
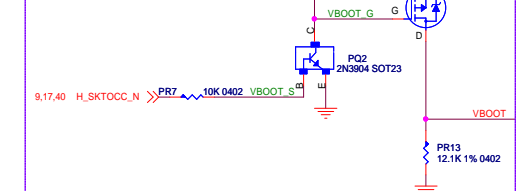
$L/DCR=R_{csp} \cdot C_{cs}$   
 $N \cdot L/DCR=R_{sw} \cdot C_{sum}$

$R_{ll}=DCR \cdot R_{droop}/R_{csn}/N$   
 $=0.8m\Omega \cdot 6.8K\Omega / 1K\Omega / 3$   
 $=1.7m\Omega$

$I_{sum}=I_{out} \cdot DCR/(N \cdot R_{sum})$



FOR POWER TEST  
VBOOT:2.56V Vout=1.1V  
0V Vout=0V



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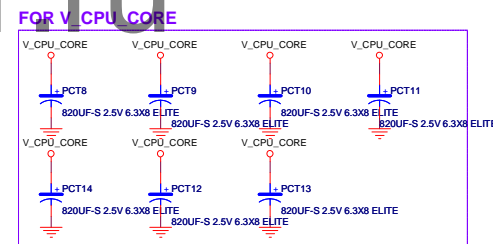
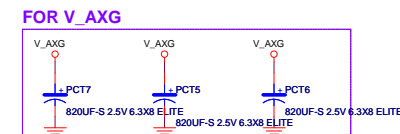
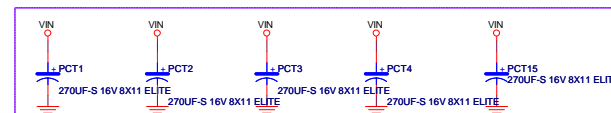
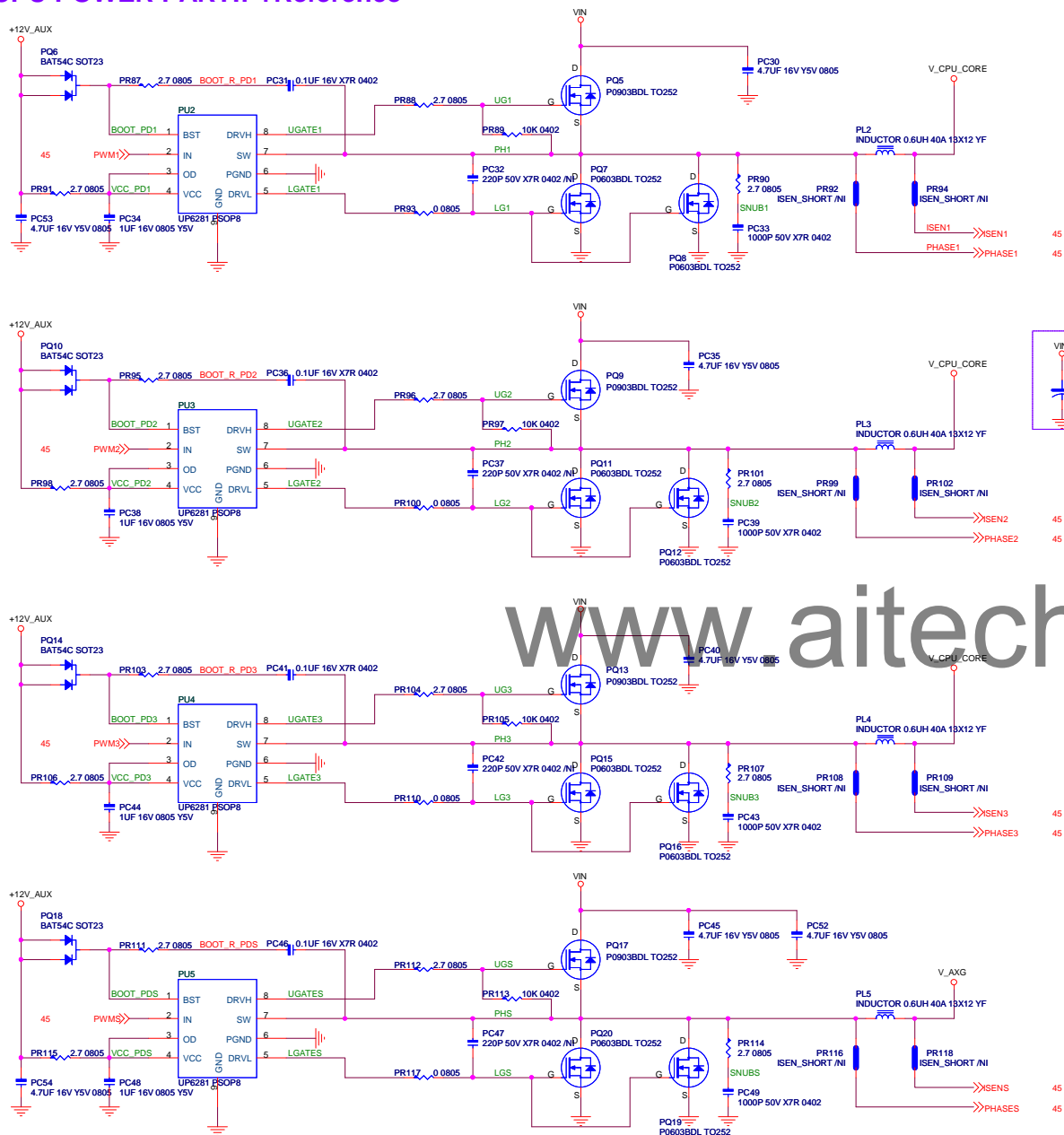
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**BIOSSTAR GROUP**

File: **VCORE VREG1**

Size: Custom Document Number: **IH61F-MHS**

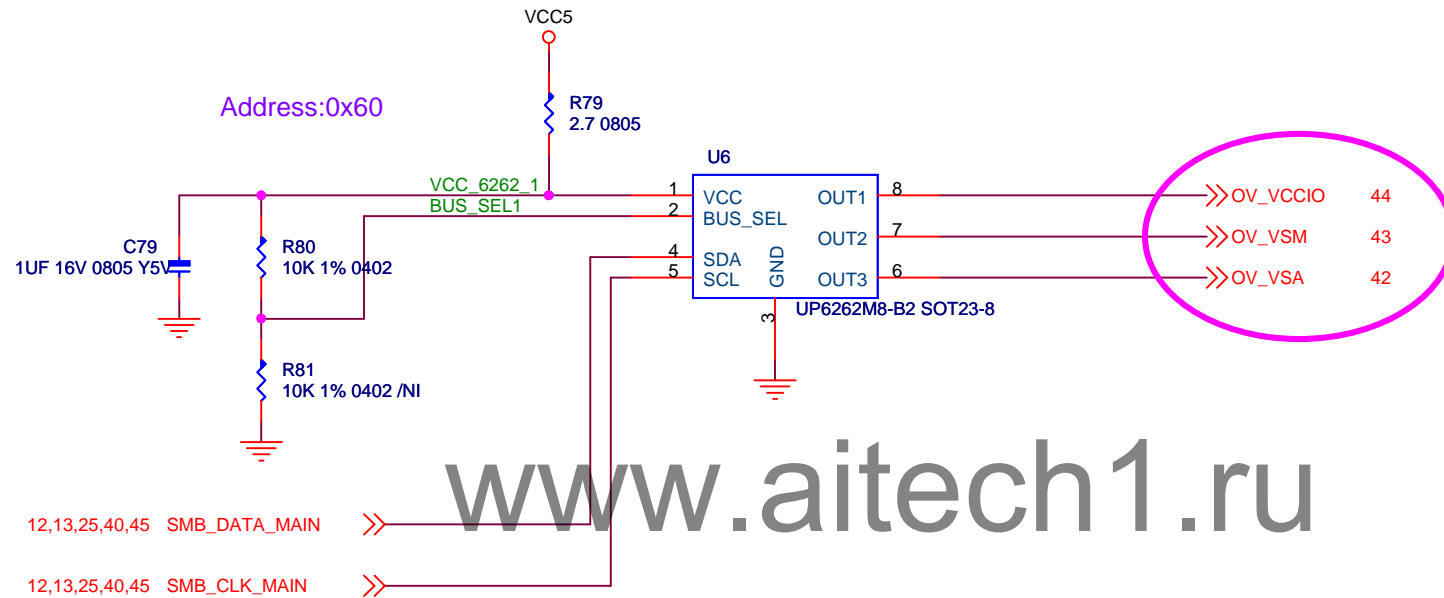
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# CPU POWER PART:P+Reference



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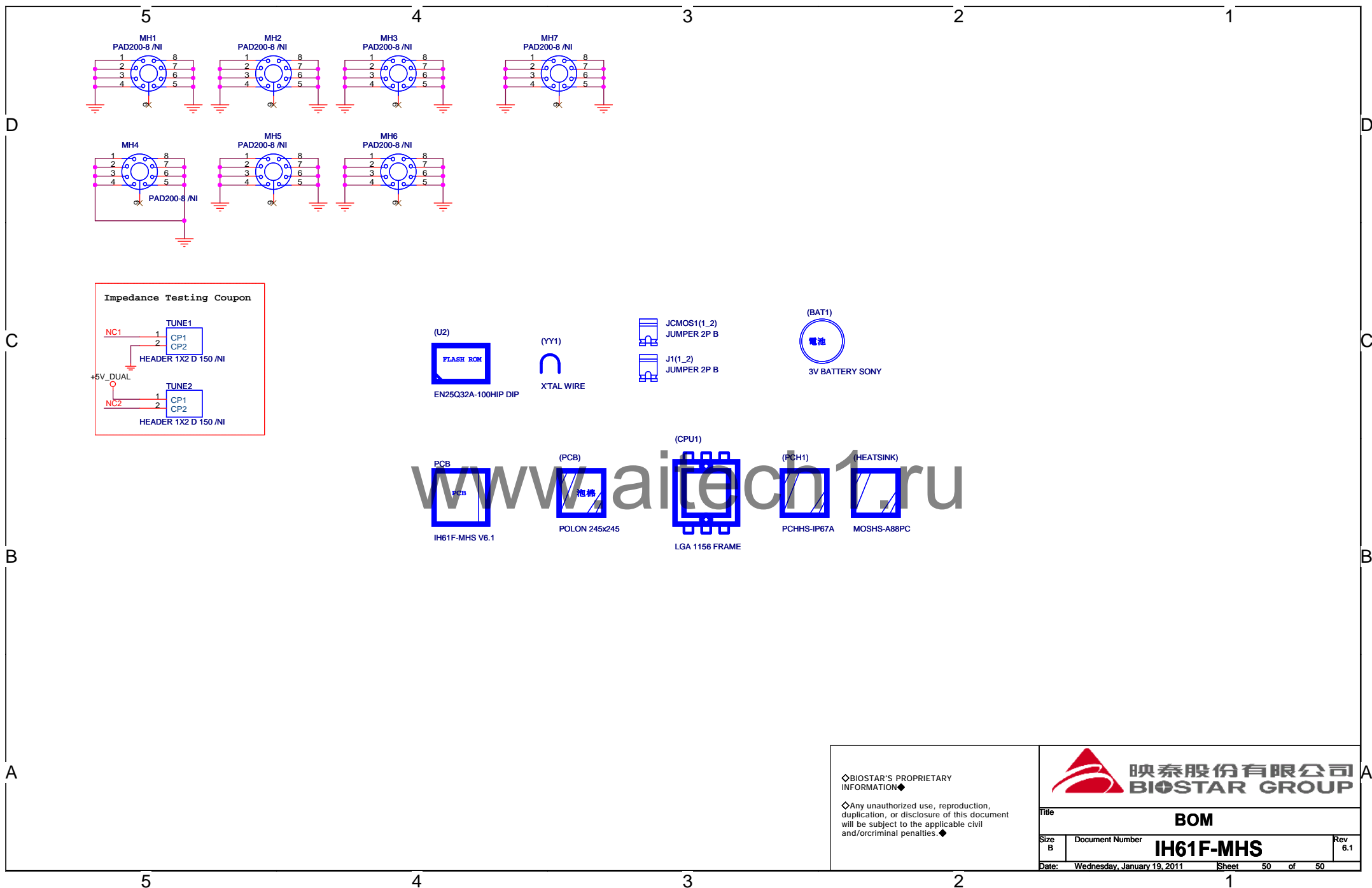
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